

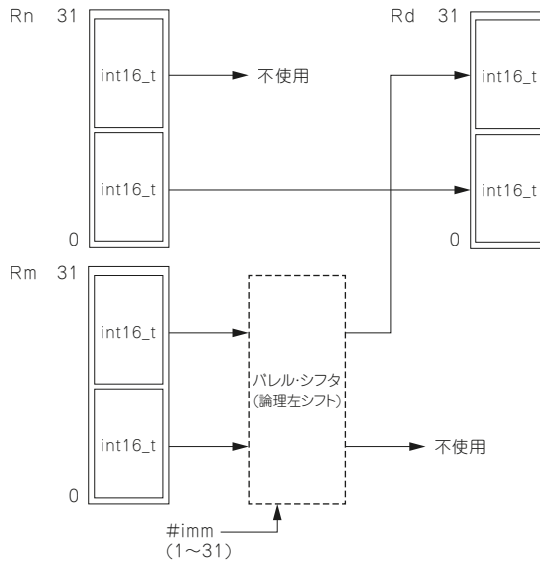
# B

## DSP命令の図解

Graphical representations of  
DSP instructions

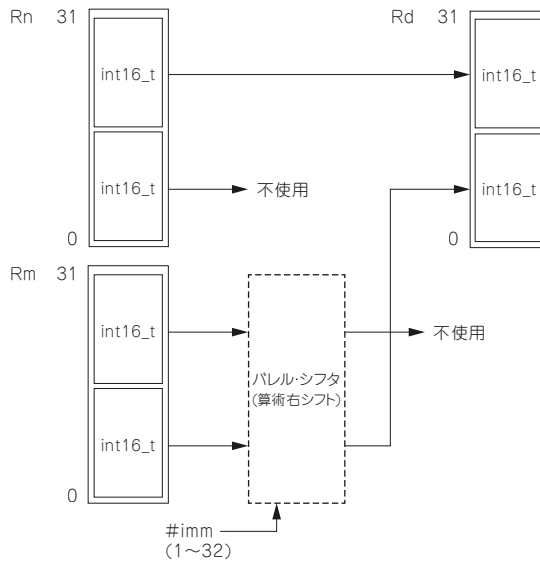
このAppendix Bには、Arm Cortex-M33プロセッサのDSP命令をグラフィカルに表現したものを掲載しています。これらの命令の説明は、5.15項「命令セット - DSP拡張」に記載されています。

PKHBT {<Rd>}, <Rn>, <Rm> {,LSL #<imm>}



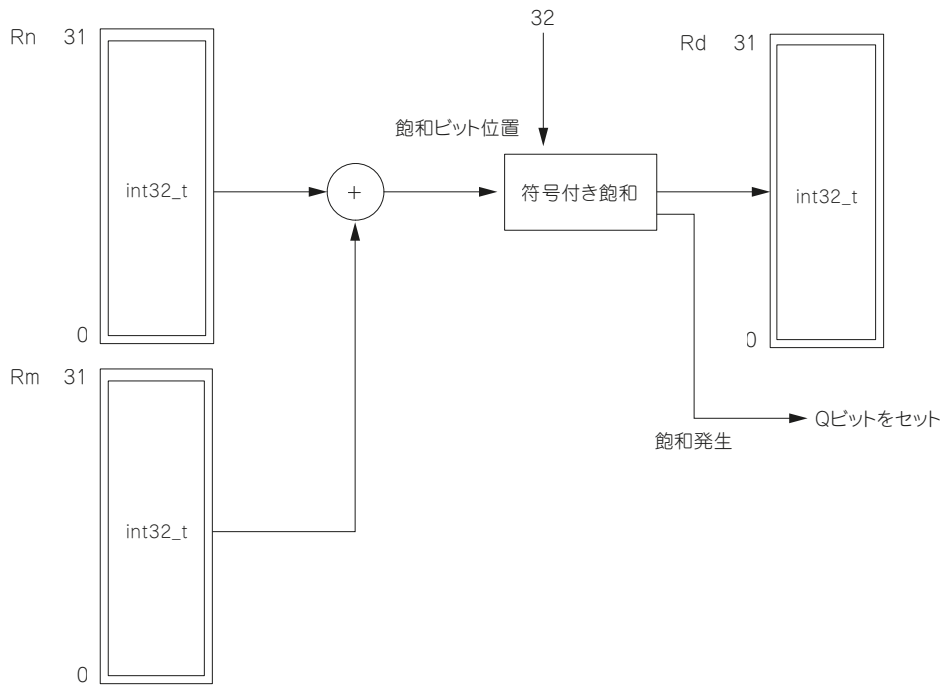
図B.1 PKHBT

PKHTB {<Rd>}, <Rn>, <Rm> {,ASR #<imm>}



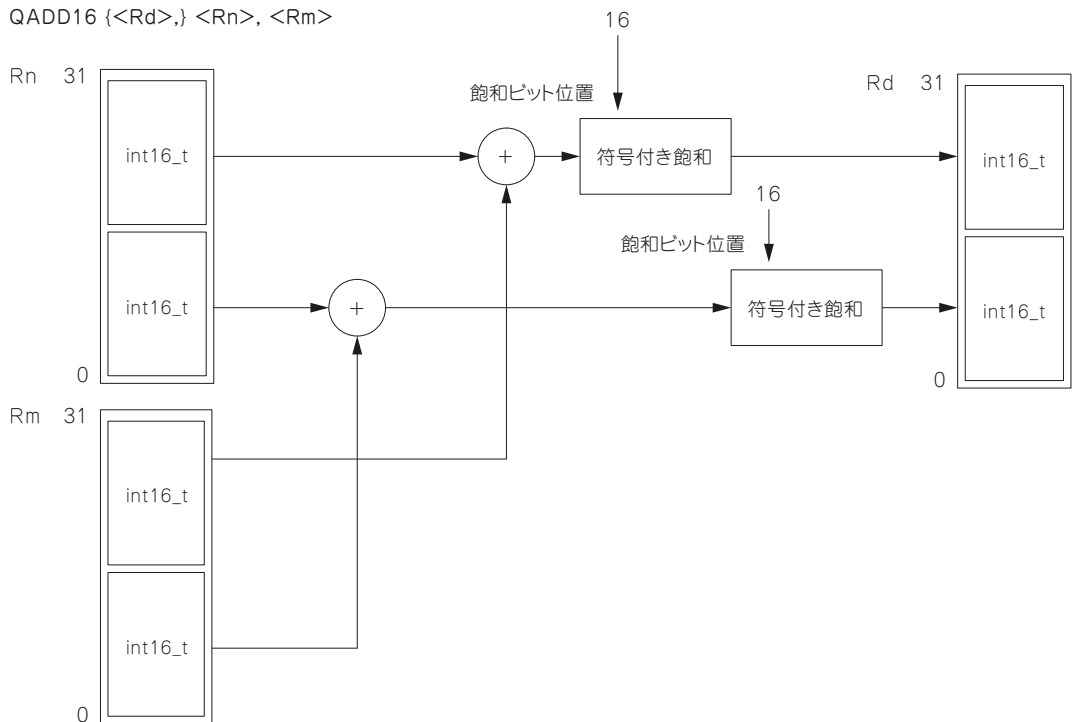
図B.2 PKHTB

QADD {<Rd>,} <Rn>, <Rm>

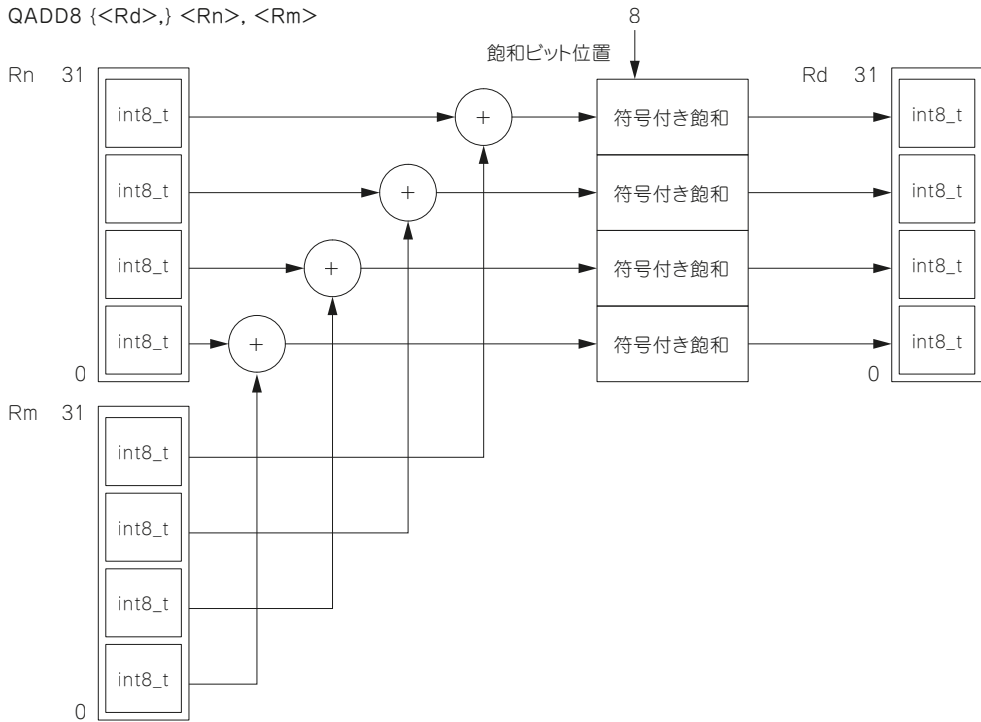


図B.3 QADD

QADD16 {<Rd>,} <Rn>, <Rm>

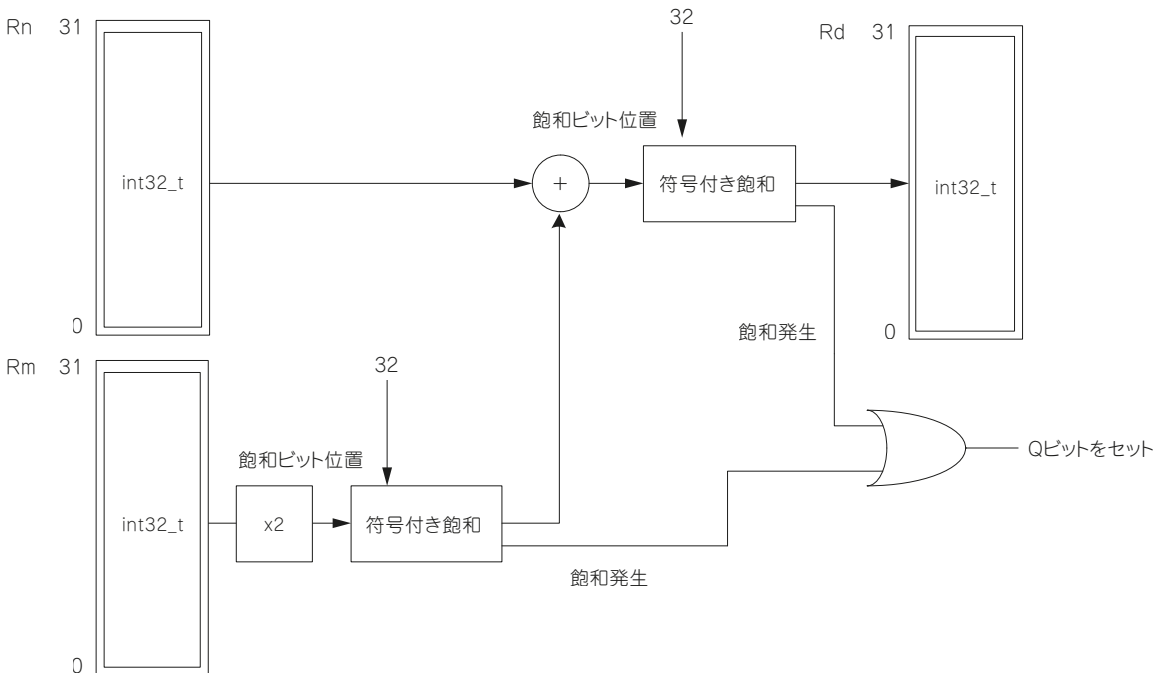


図B.4 QADD16



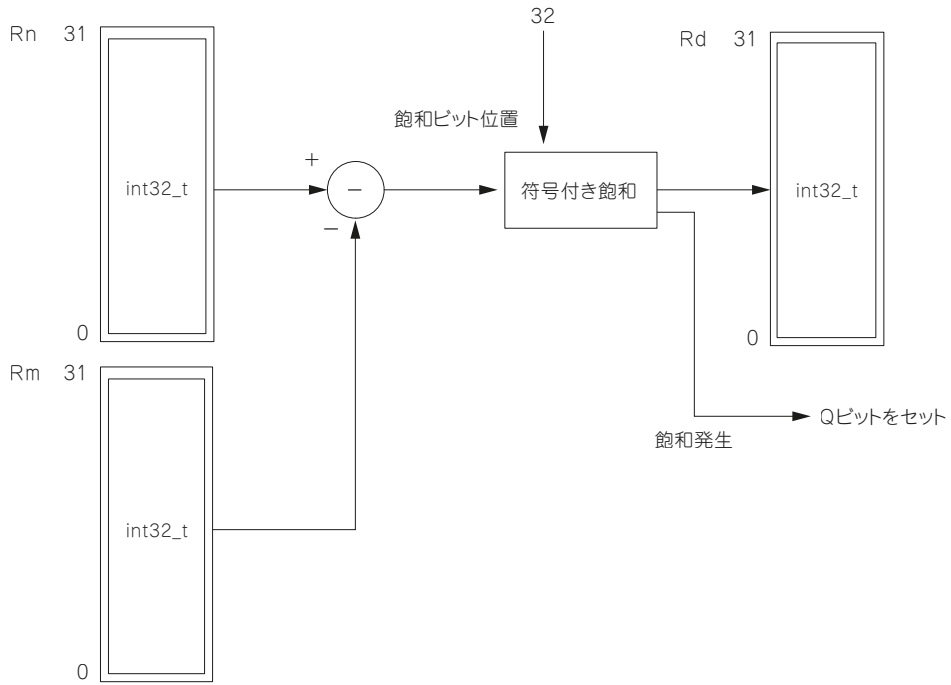
図B.5 QADD8

QDADD {<Rd>,} <Rn>, <Rm>



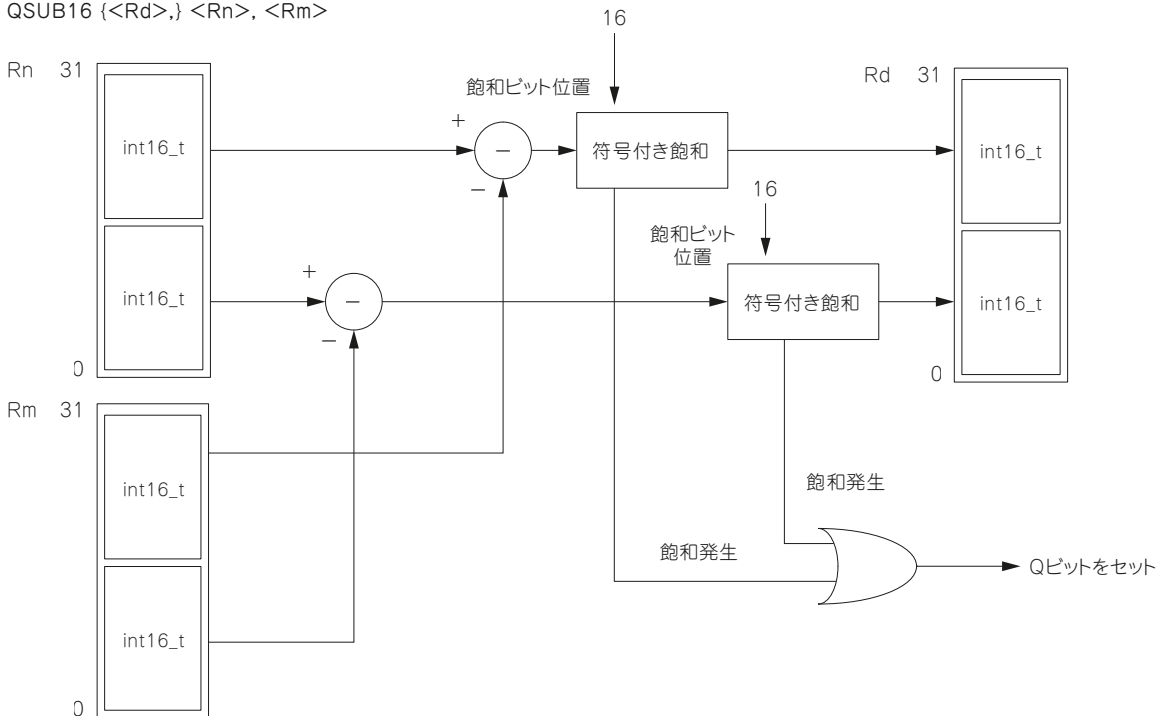
図B.6 QDADD

QSUB (<Rd>,) <Rn>, <Rm>

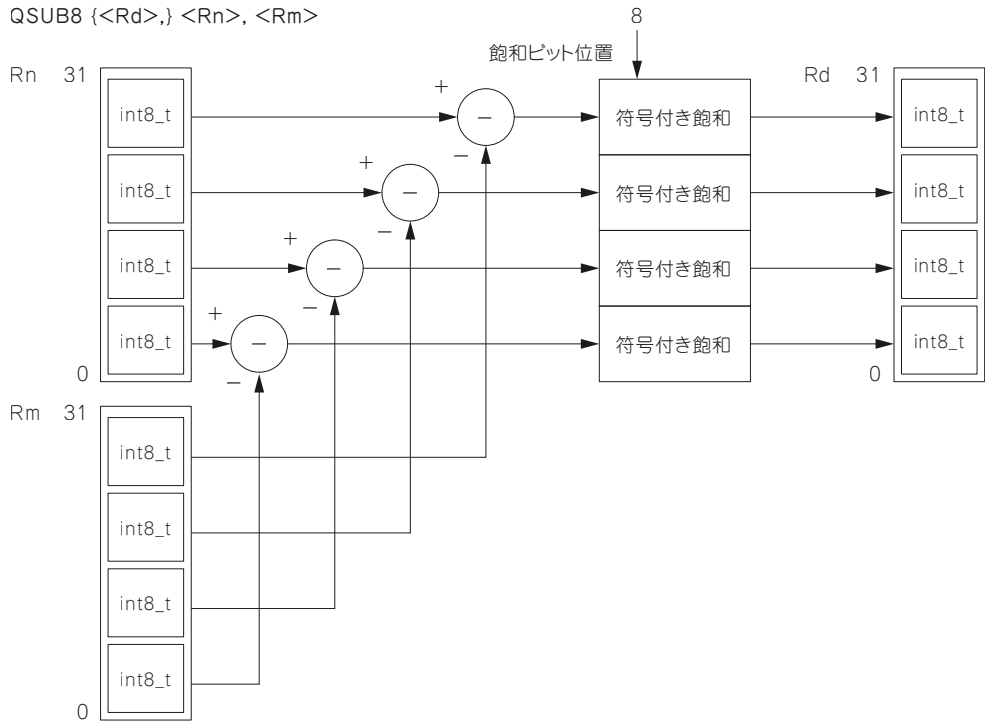


図B.7 QSUB

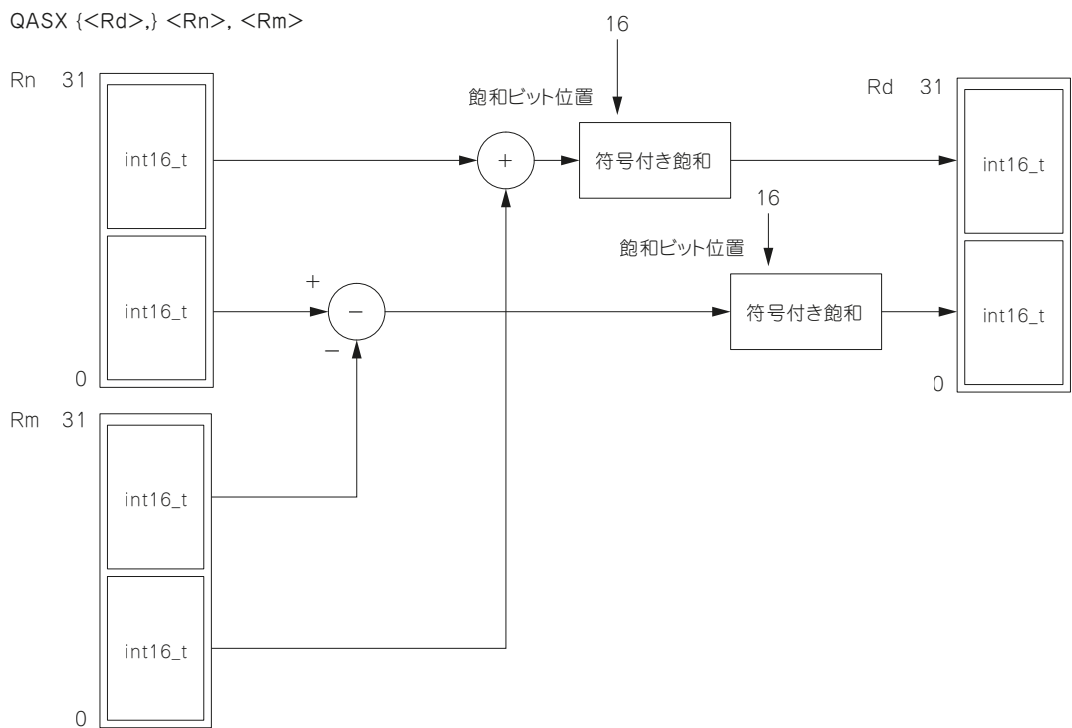
QSUB16 (<Rd>,) <Rn>, <Rm>



図B.8 QSUB16

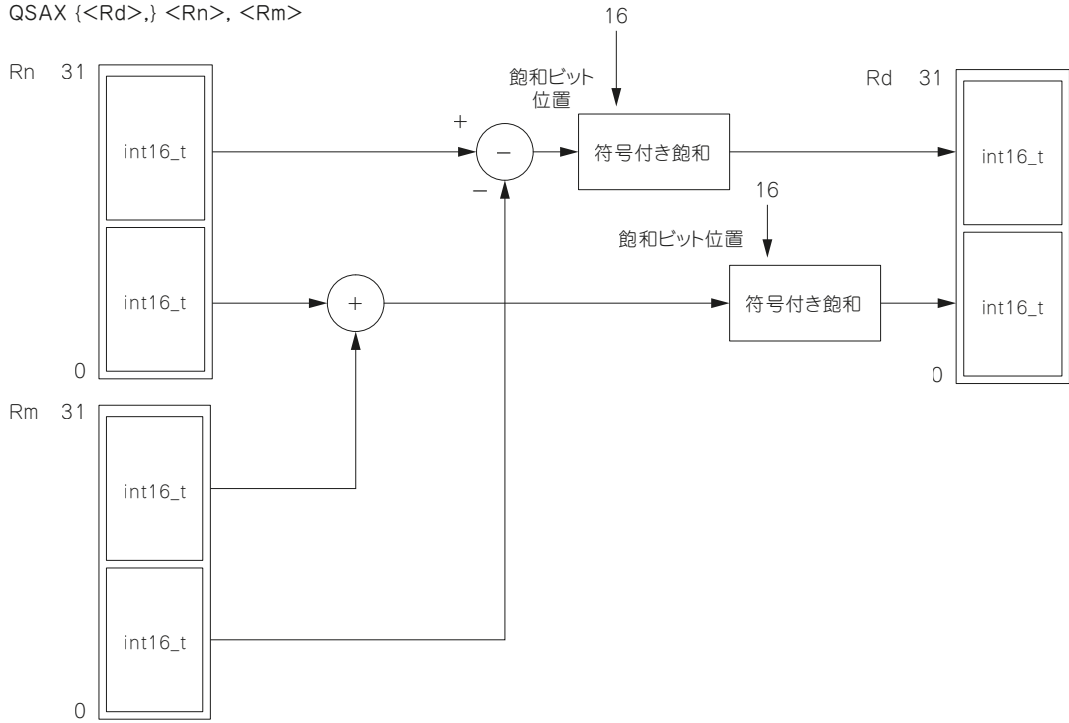


図B.9 QSUB8



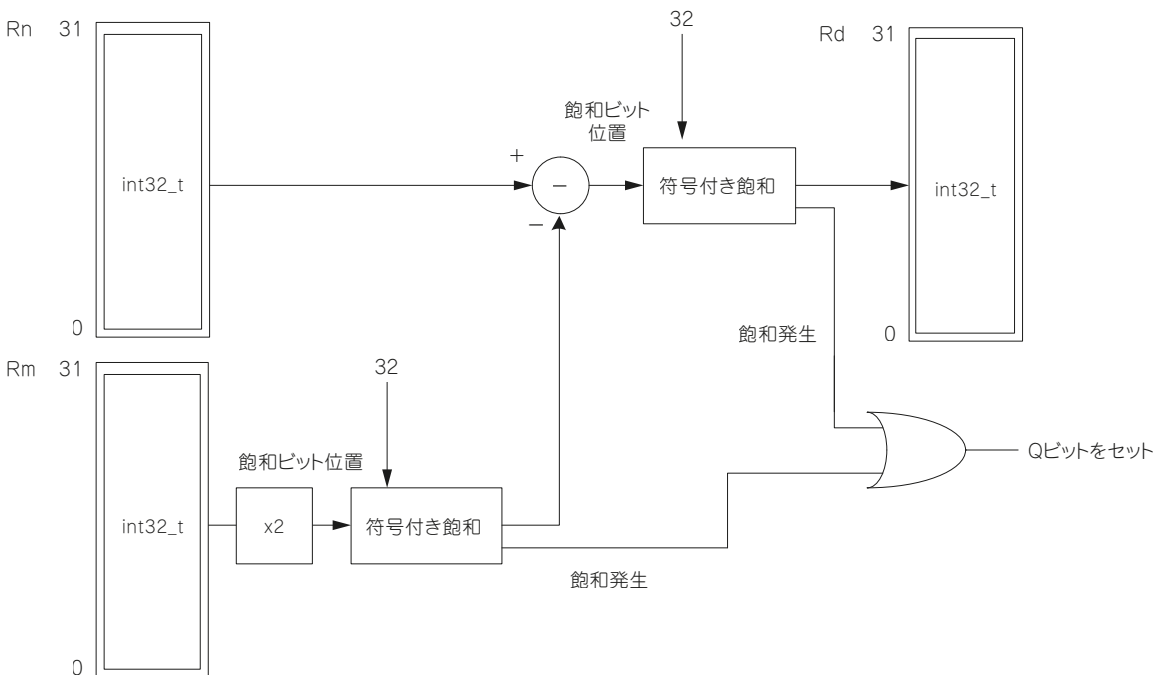
図B.10 QASX

QSAX {<Rd>,<Rn>, <Rm>



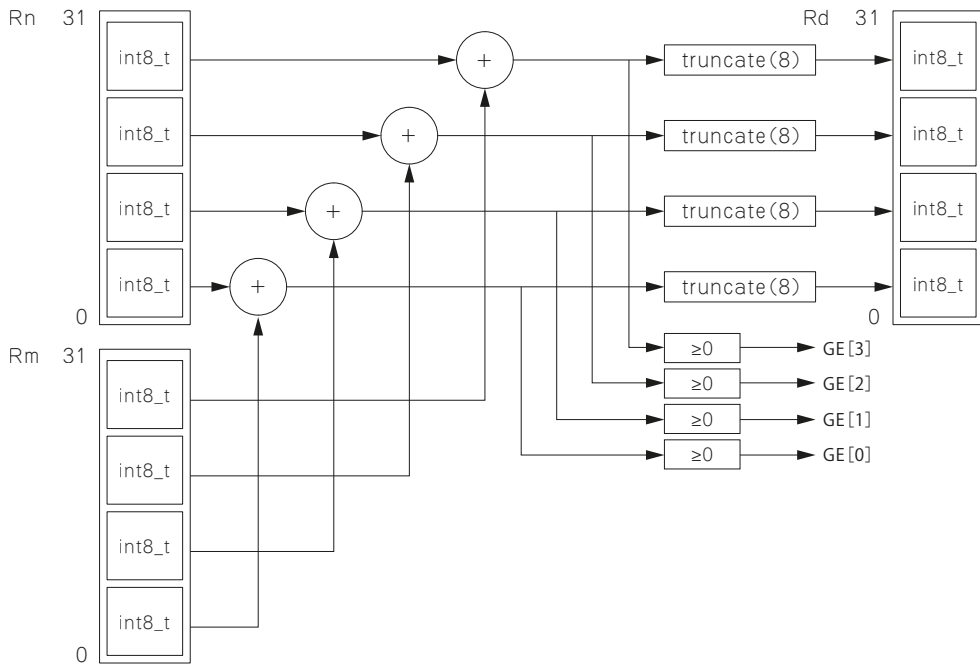
図B.11 QSAX

QDSUB {<Rd>,<Rn>, <Rm>



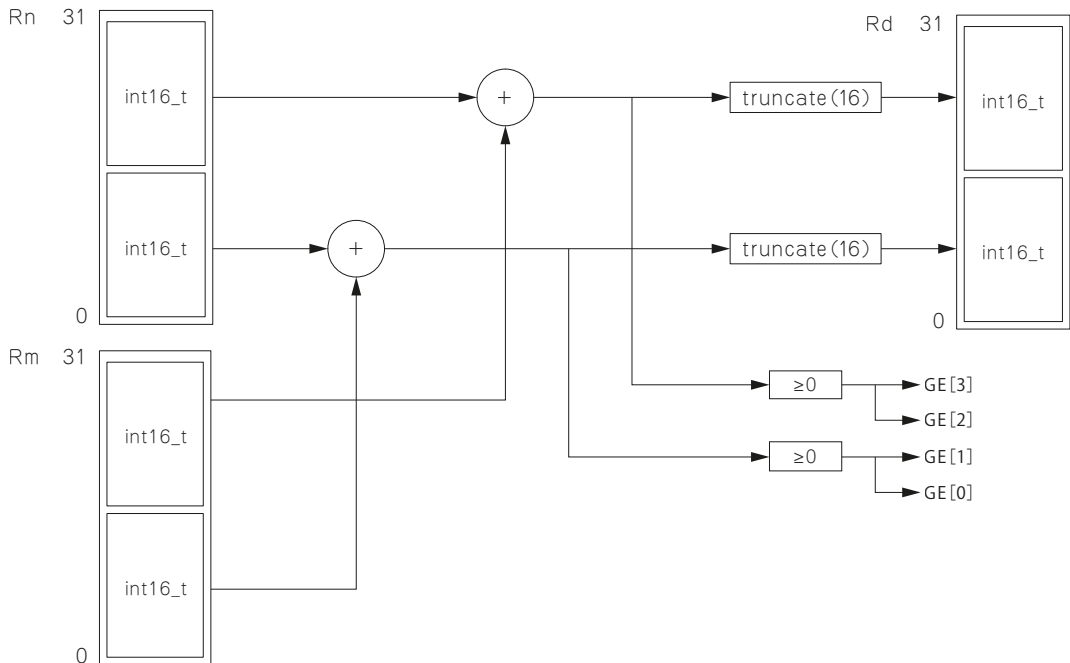
図B.12 QDSUB

SADD8 {<Rd>,} <Rn>, <Rm>



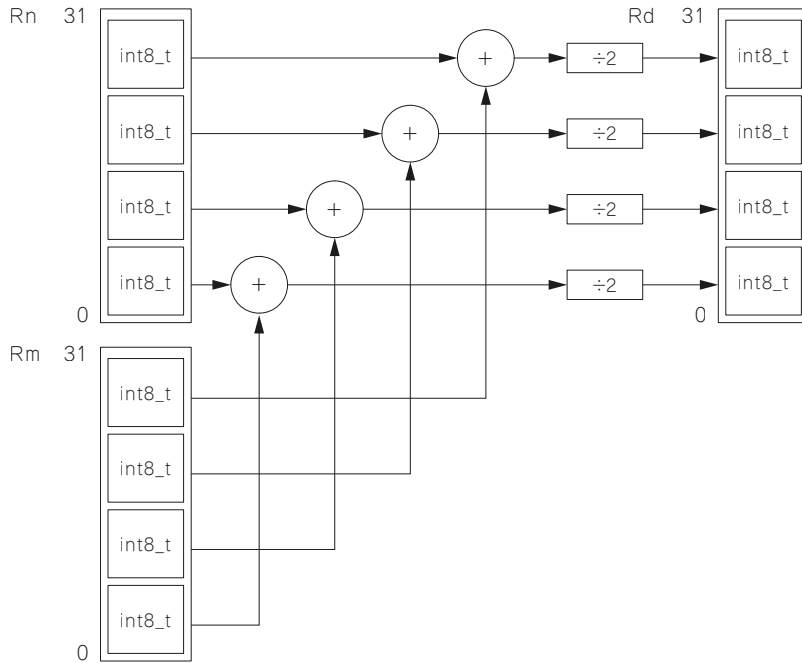
図B.13 SADD8

SADD16 {<Rd>,} <Rn>, <Rm>



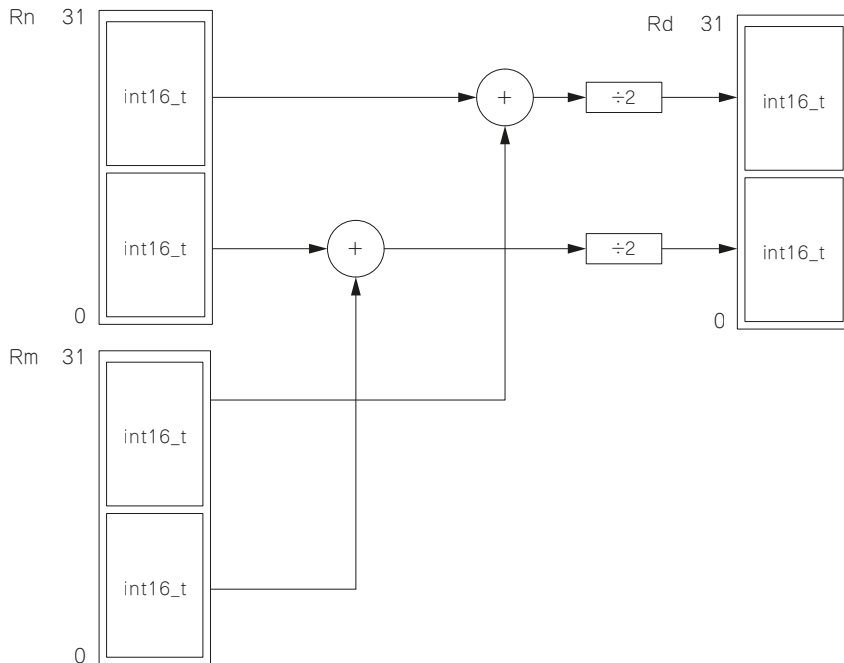
図B.14 SADD16

SHADD8 (<Rd>,) <Rn>, <Rm>



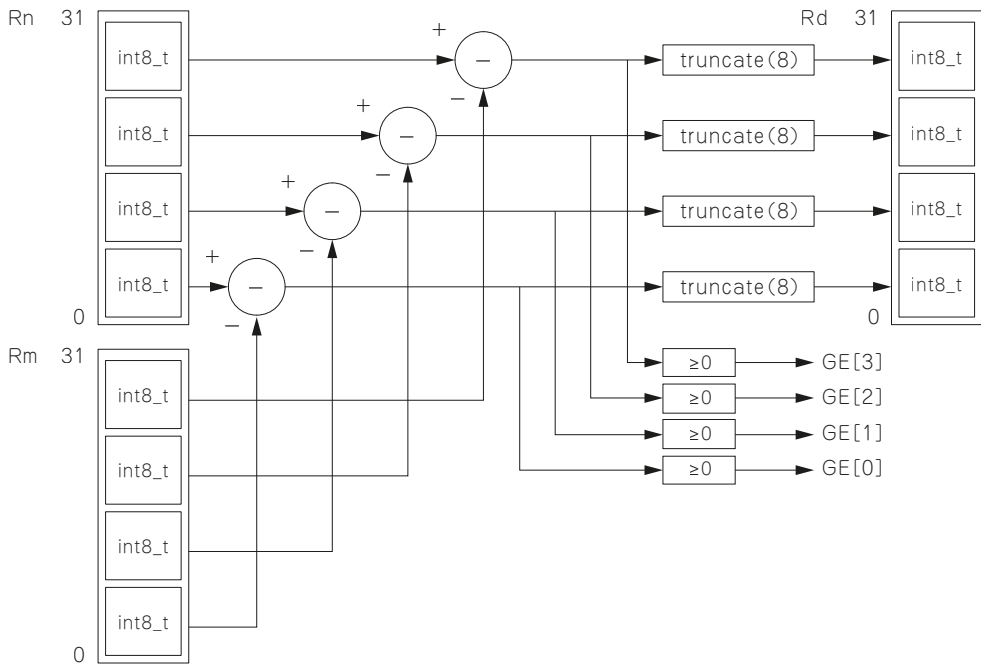
図B.15 SHADD8

SHADD16 (<Rd>,) <Rn>, <Rm>



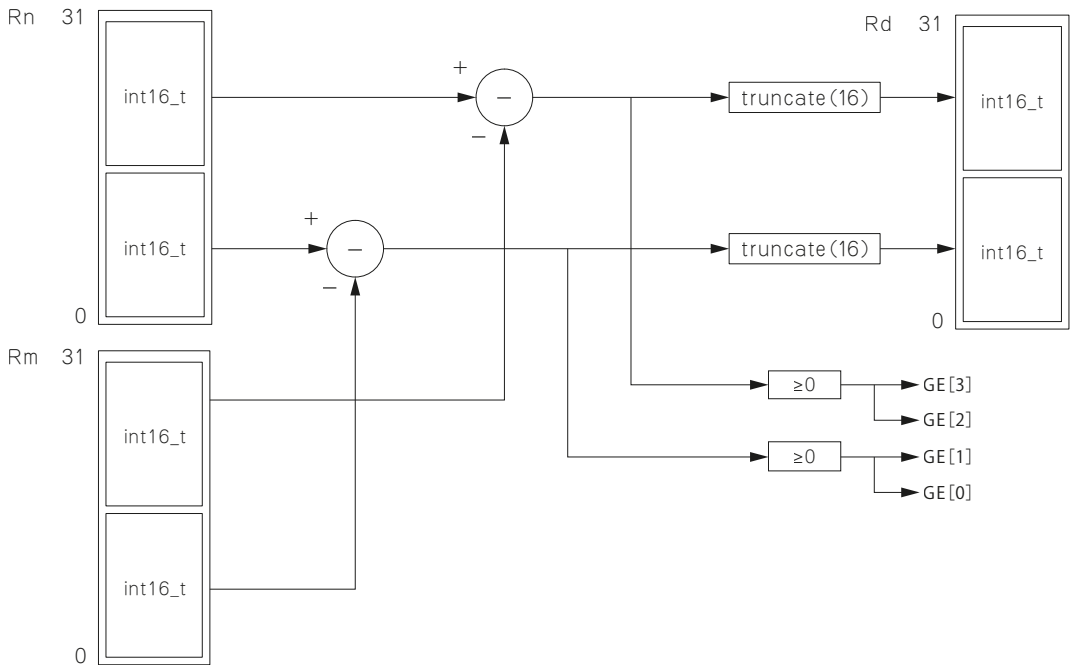
図B.16 SHADD16

SSUB8 {<Rd>,} <Rn>, <Rm>



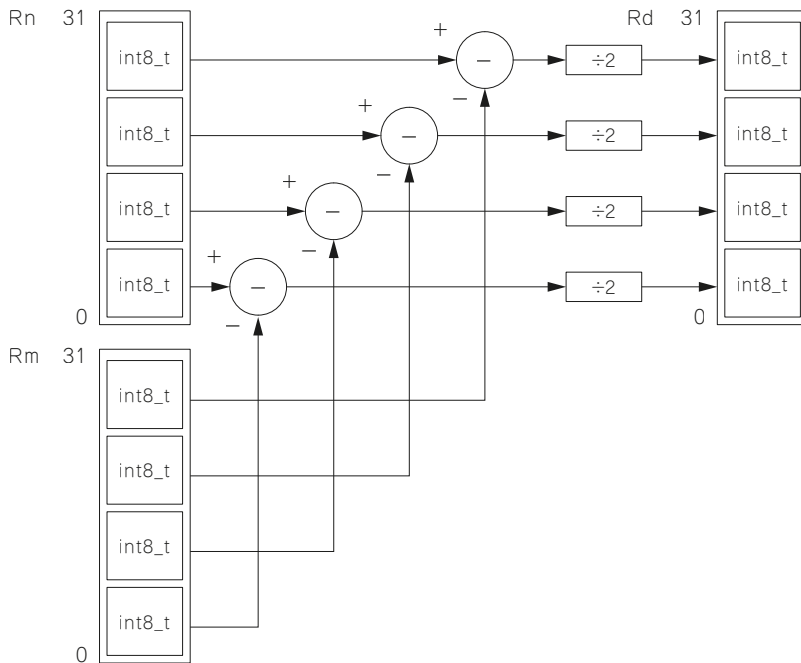
図B.17 SSUB8

SSUB16 {<Rd>,} <Rn>, <Rm>



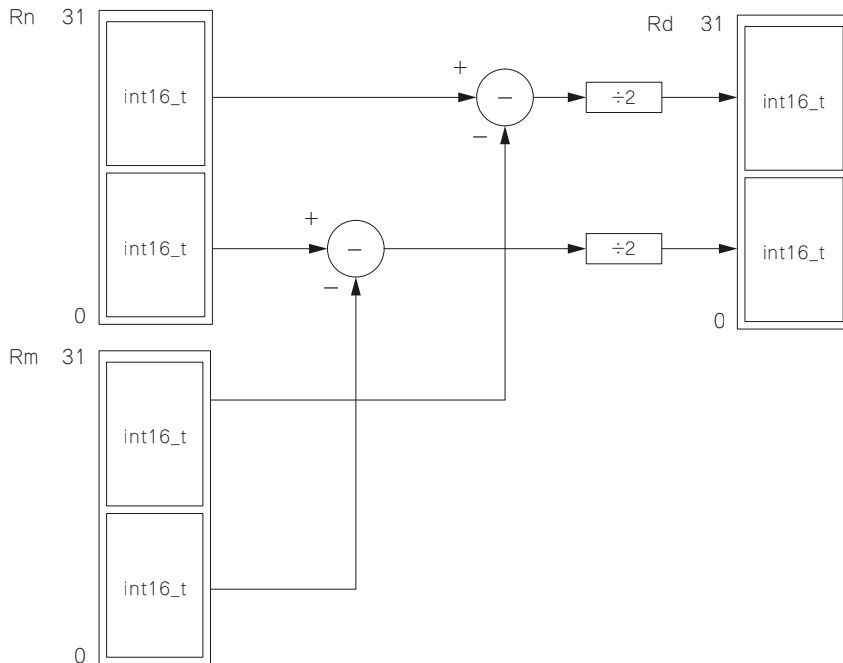
図B.18 SSUB16

SHSUB8 (<Rd>,) <Rn>, <Rm>



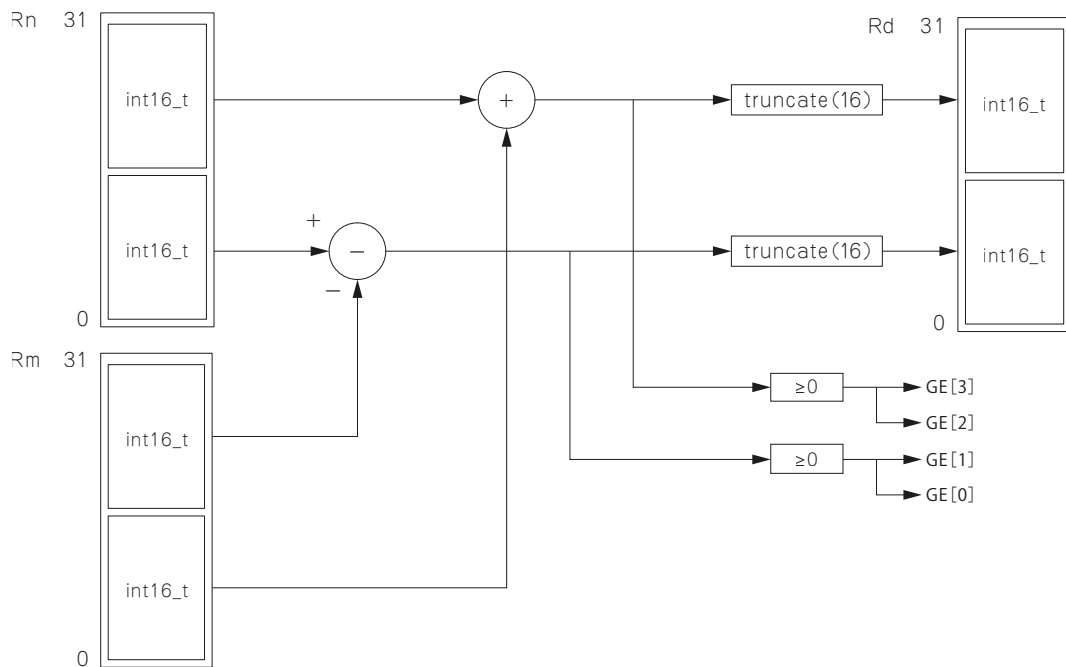
図B.19 SHSUB8

SHSUB16 (<Rd>,) <Rn>, <Rm>



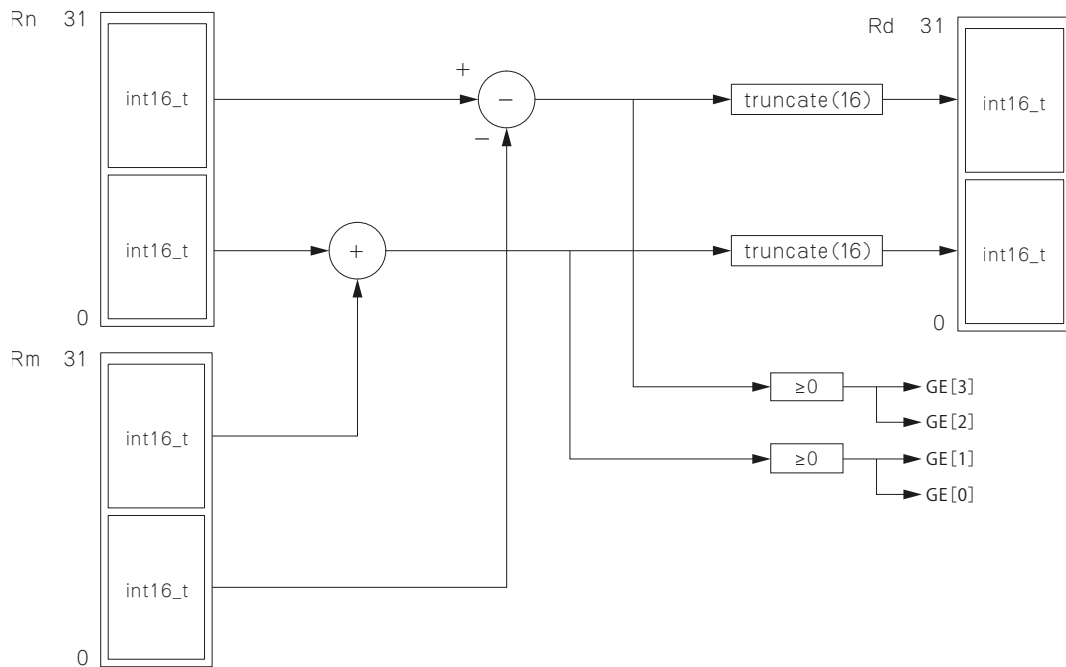
図B.20 SHSUB16

SASX {<Rd>}, <Rn>, <Rm>



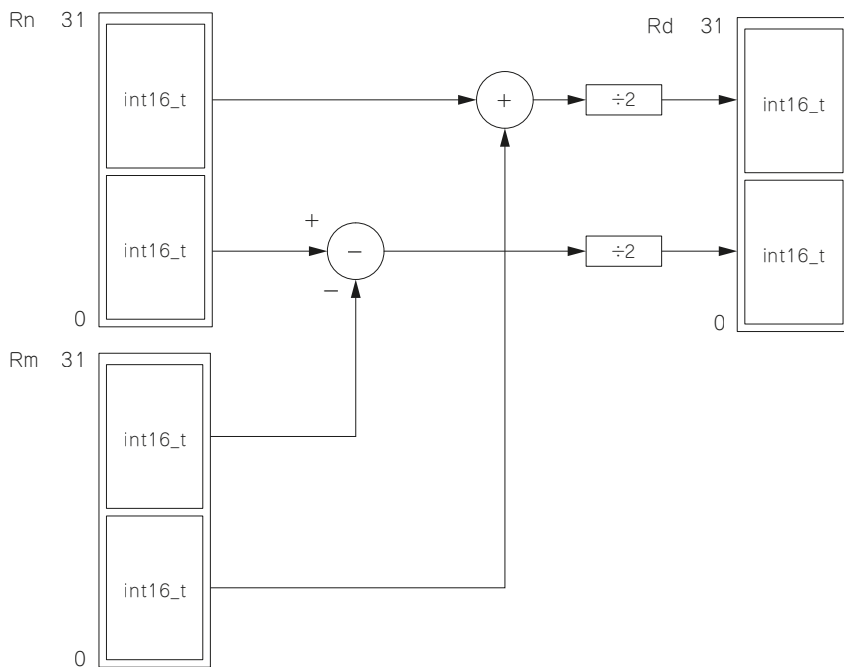
図B.21 SASX

SSAX {<Rd>}, <Rn>, <Rm>



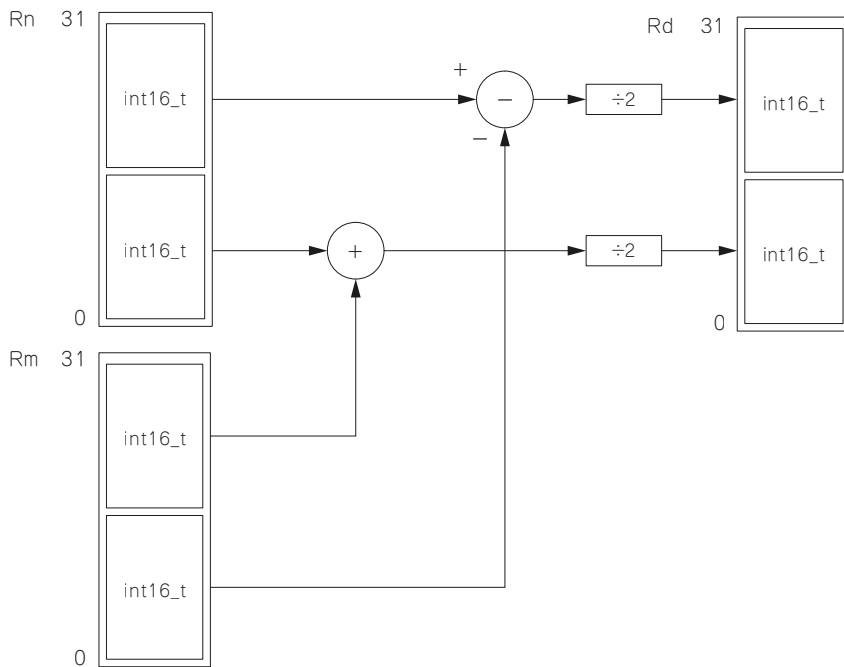
図B.22 SSAX

SHASX {<Rd>,} <Rn>, <Rm>

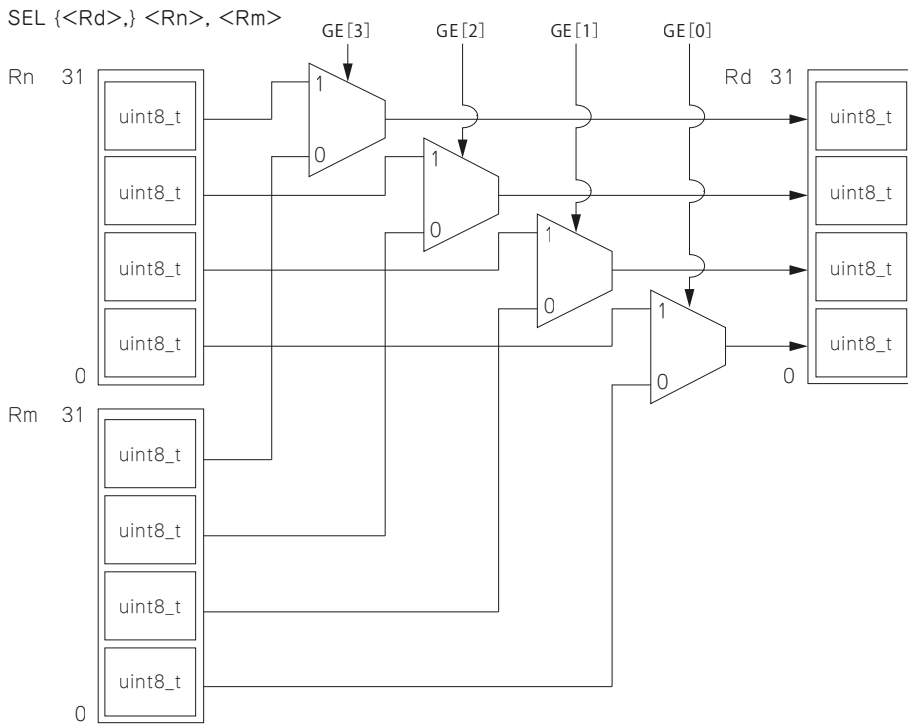


図B.23 SHASX

SHSAX {<Rd>,} <Rn>, <Rm>

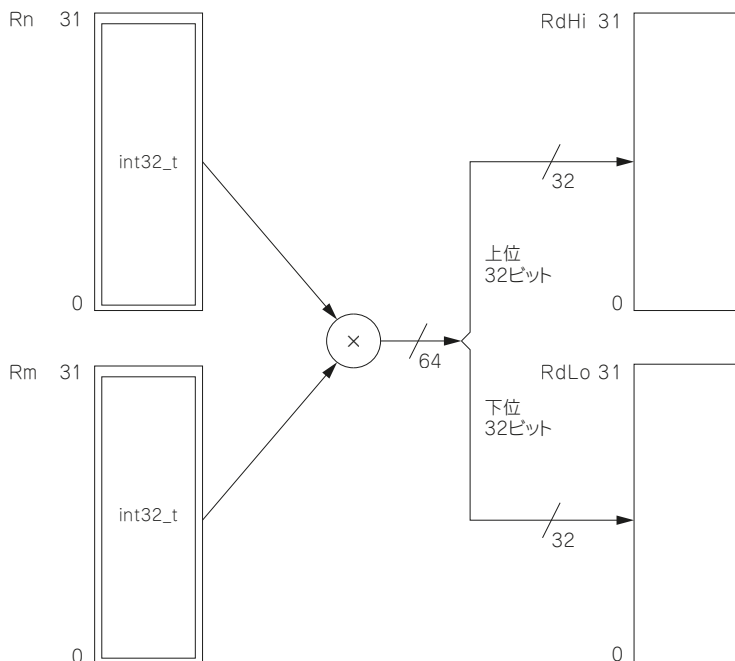


図B.24 SHSAX



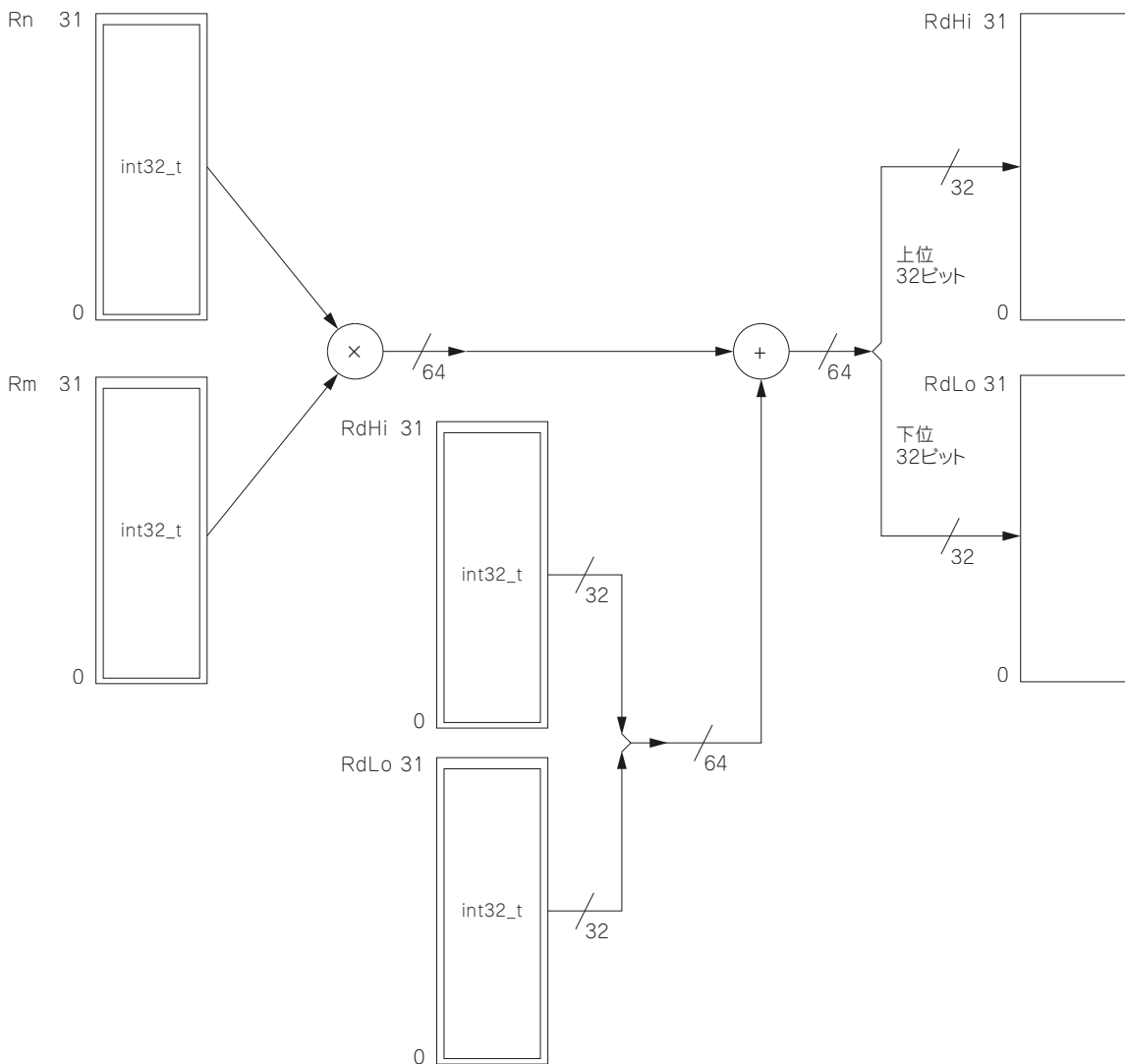
図B.25 SEL

SMULL <RdLo>, <RdHi>, <Rn>, <Rm>  
 (DSP拡張が実装されていない場合でもCortex-M33プロセッサで利用可能)



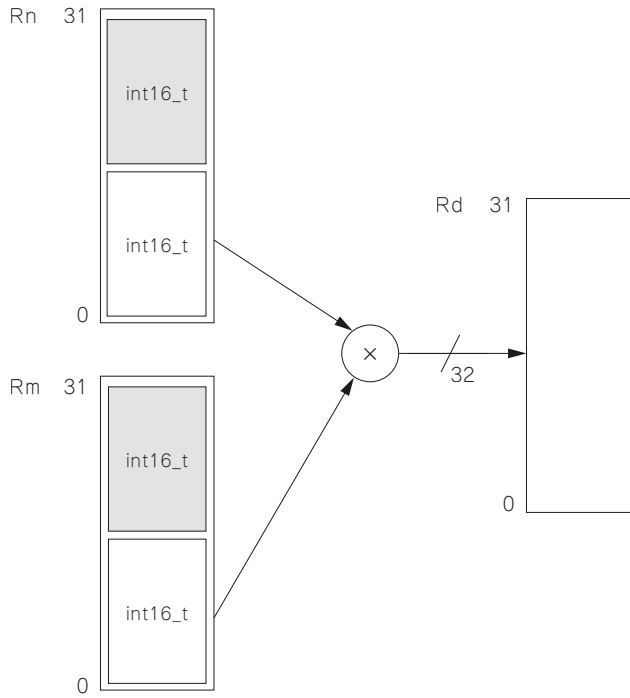
図B.26 SMULL

SMLAL <RdLo>, <RdHi>, <Rn>, <Rm>  
 (DSP拡張が実装されていなくてもCortex-M33プロセッサで利用可能)



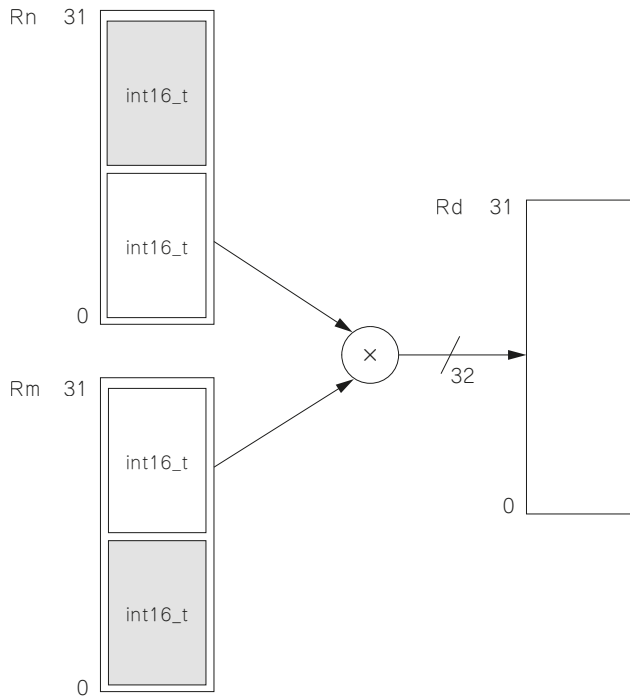
図B.27 SMLAL

SMULBB {<Rd>,} <Rn>, <Rm>



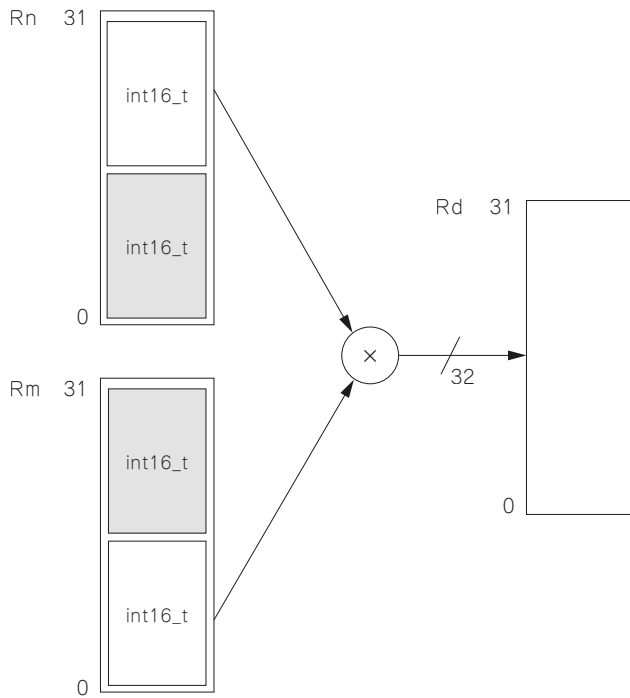
図B.28 SMULBB

SMULBT {<Rd>,} <Rn>, <Rm>



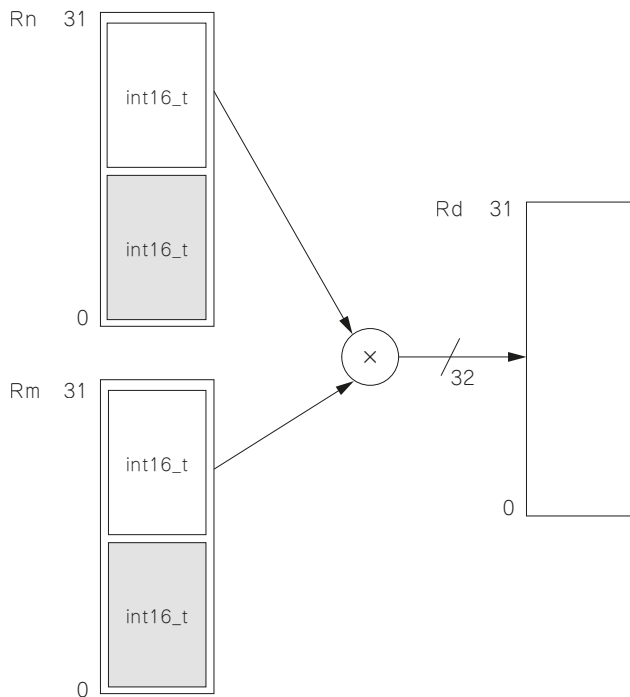
図B.29 SMULBT

SMULTB {<Rd>,} <Rn>, <Rm>



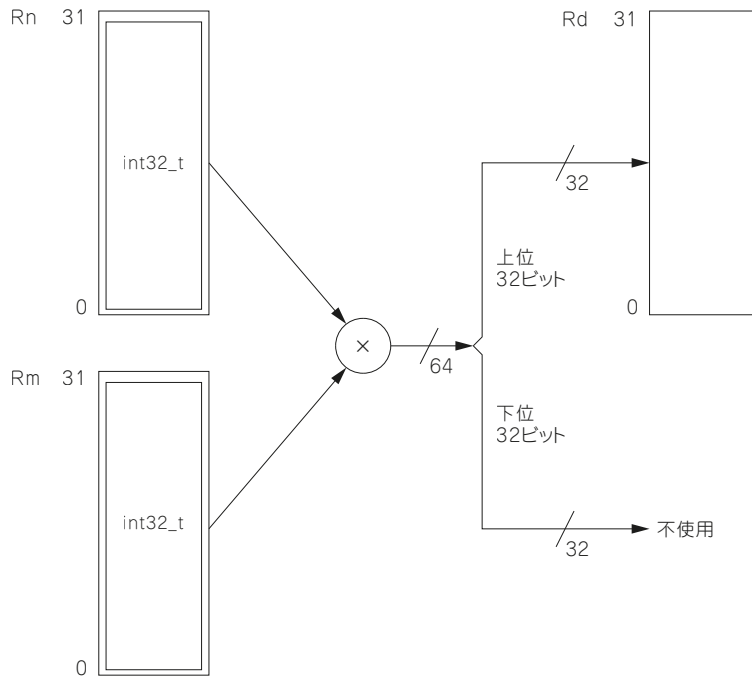
図B.30 SMULTB

SMULTT {<Rd>,} <Rn>, <Rm>



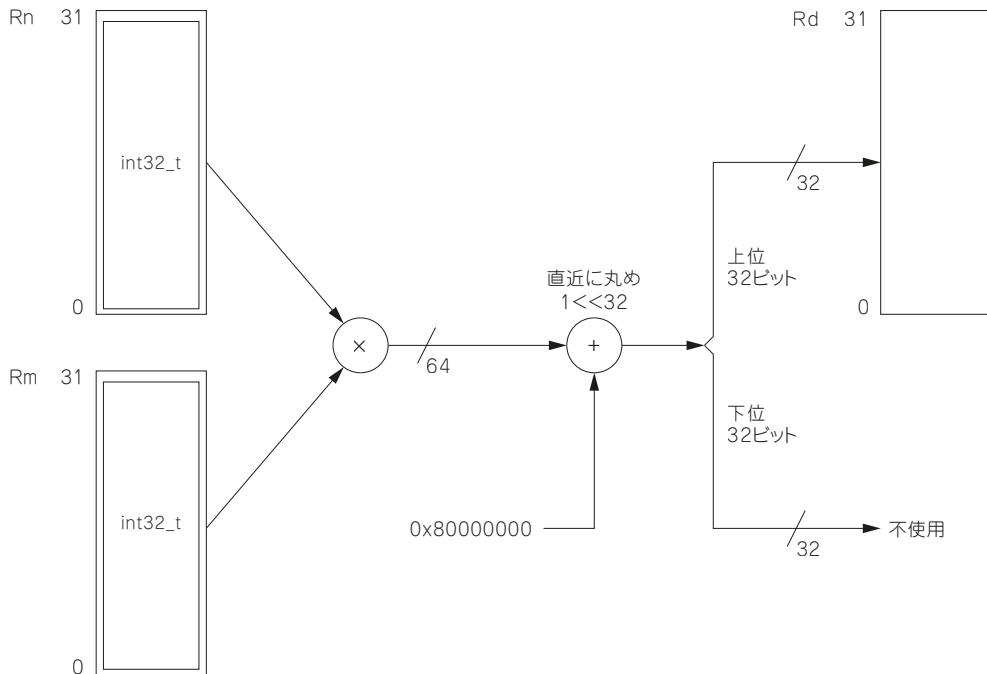
図B.31 SMULTT

SMMUL {<Rd>,} <Rn>, <Rm>



図B.32 SMMUL

SMMULR {<Rd>,} <Rn>, <Rm>



図B.33 SMMULR

SMMLA <Rd>, <Rn>, <Rm>, <Ra>

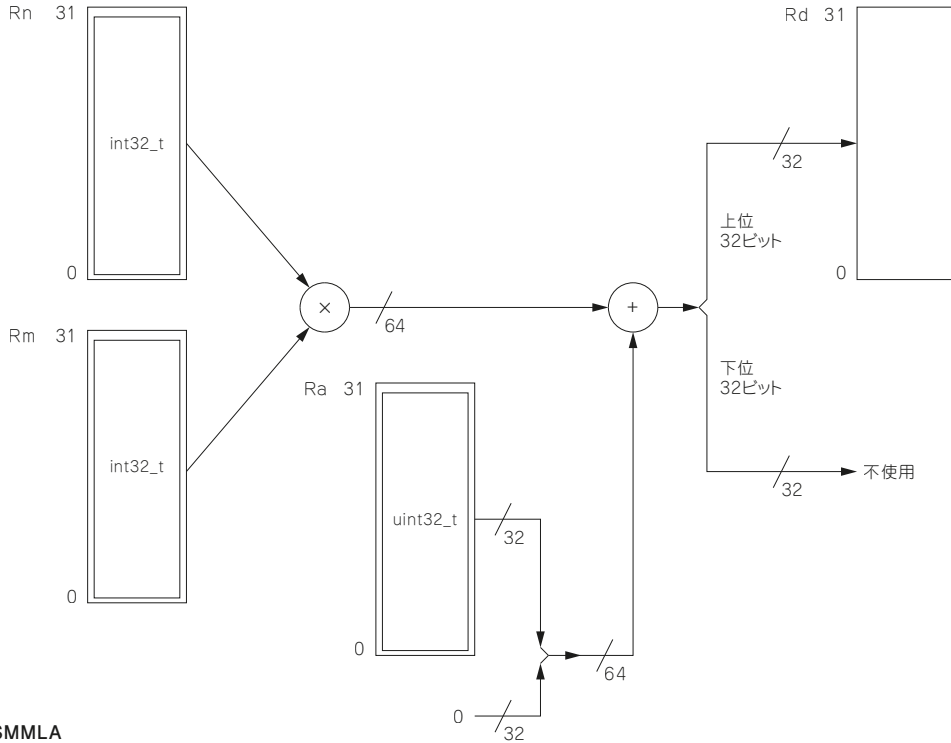


図 B.34 SMMLA

SMMLAR <Rd>, <Rn>, <Rm>, <Ra>

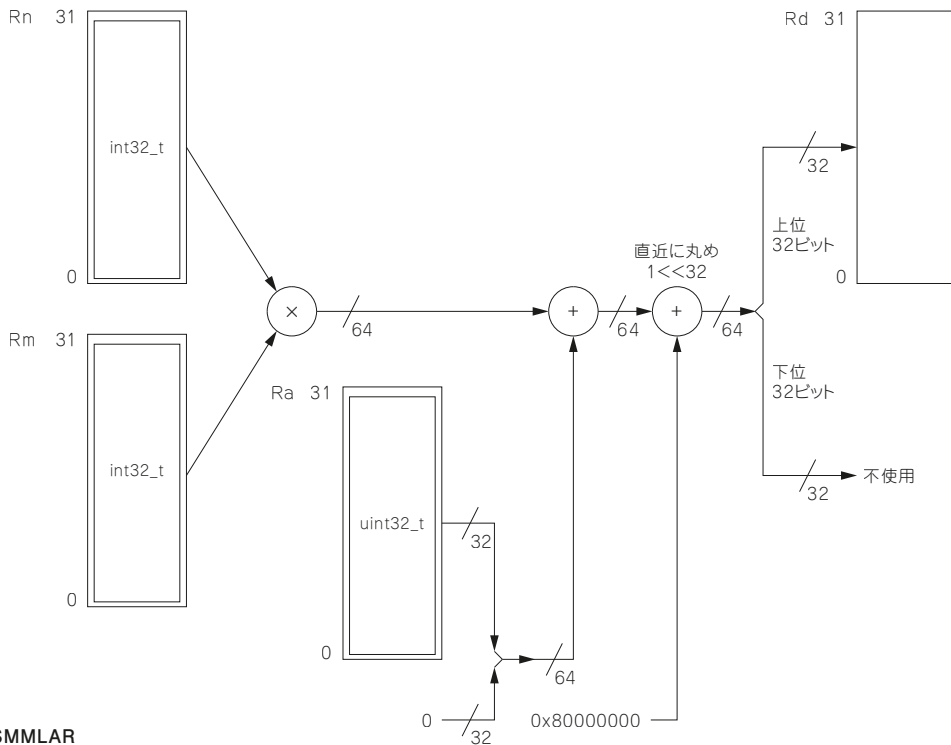
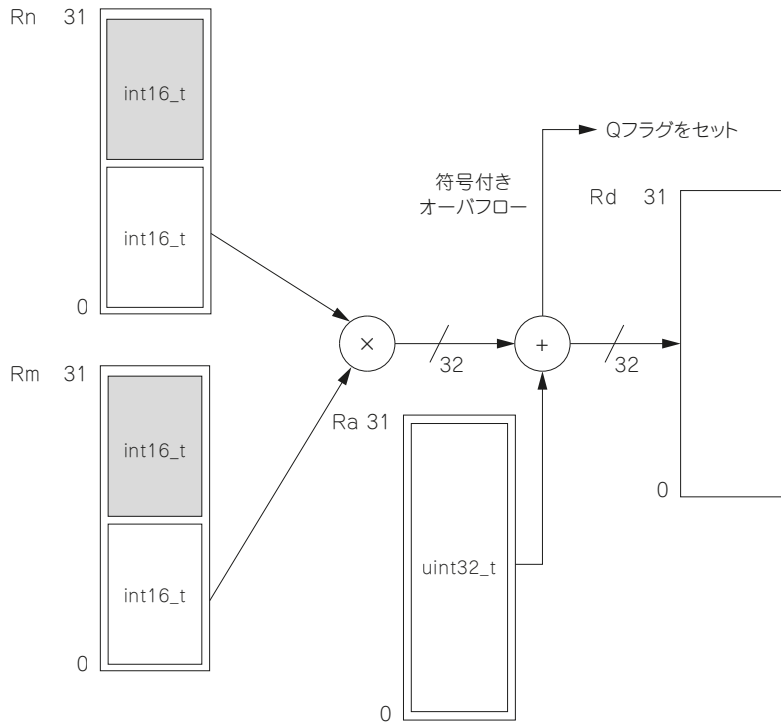


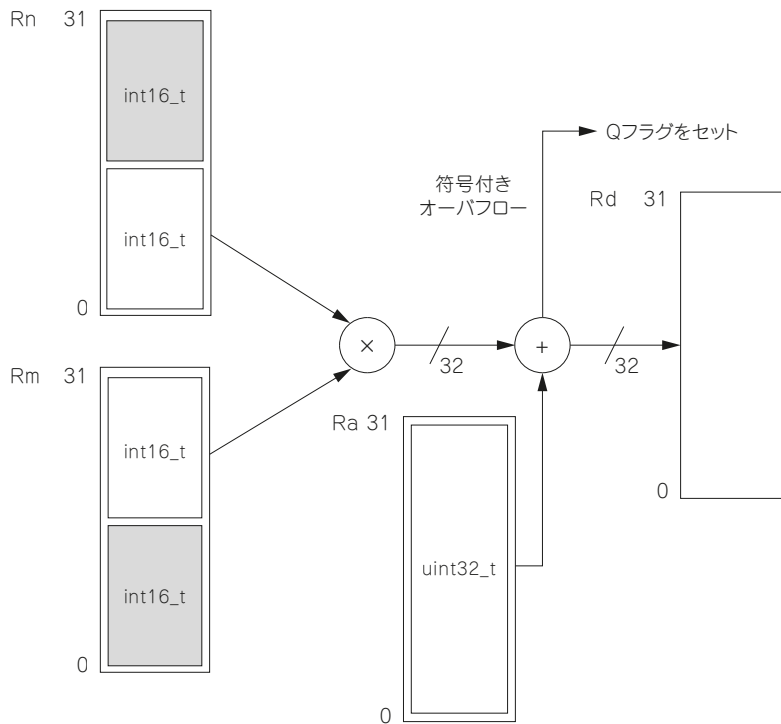
図 B.35 SMMLAR

SMLABB <Rd>, <Rn>, <Rm>, <Ra>



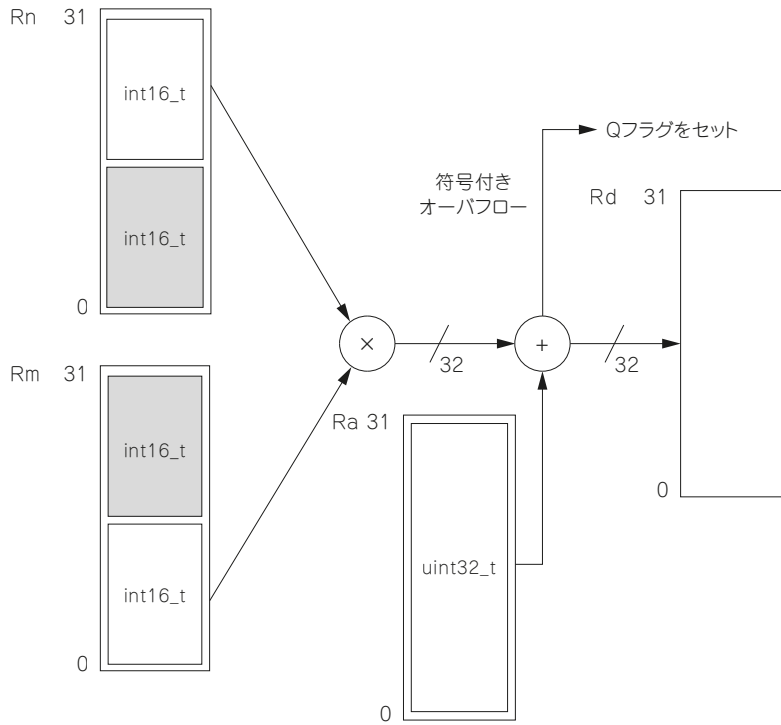
図B.36 SMLABB

SMLABT <Rd>, <Rn>, <Rm>, <Ra>



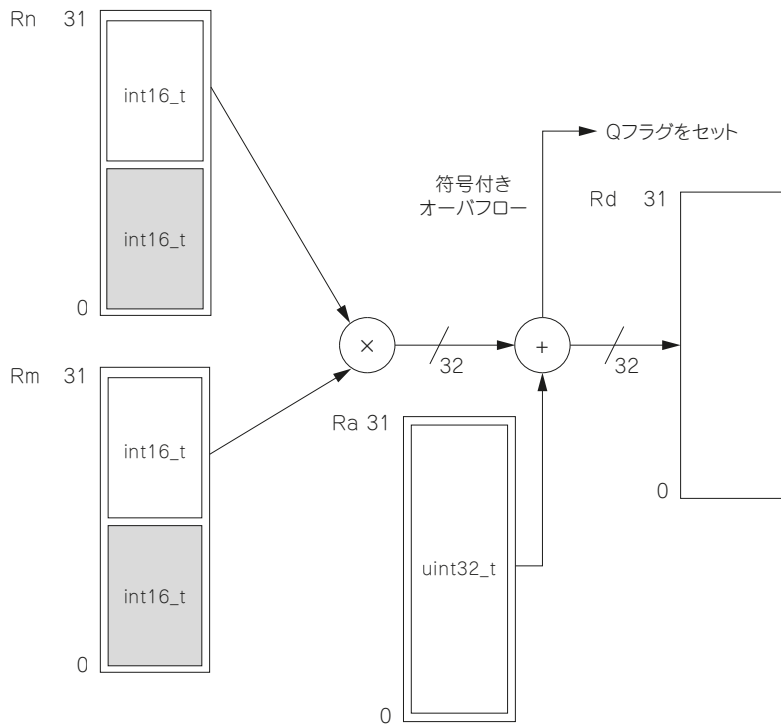
図B.37 SMLABT

SMLATB <Rd>, <Rn>, <Rm>, <Ra>



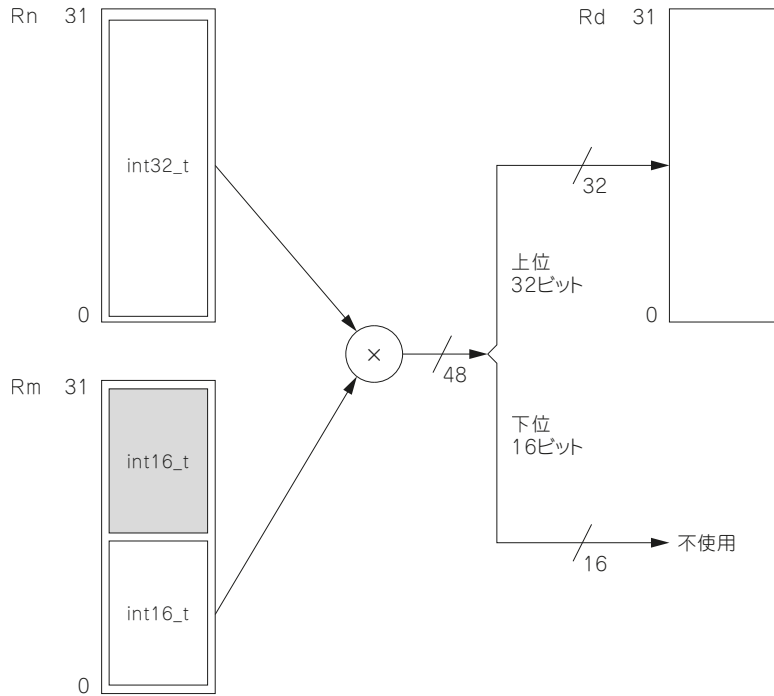
図B.38 SMLATB

SMLATT <Rd>, <Rn>, <Rm>, <Ra>



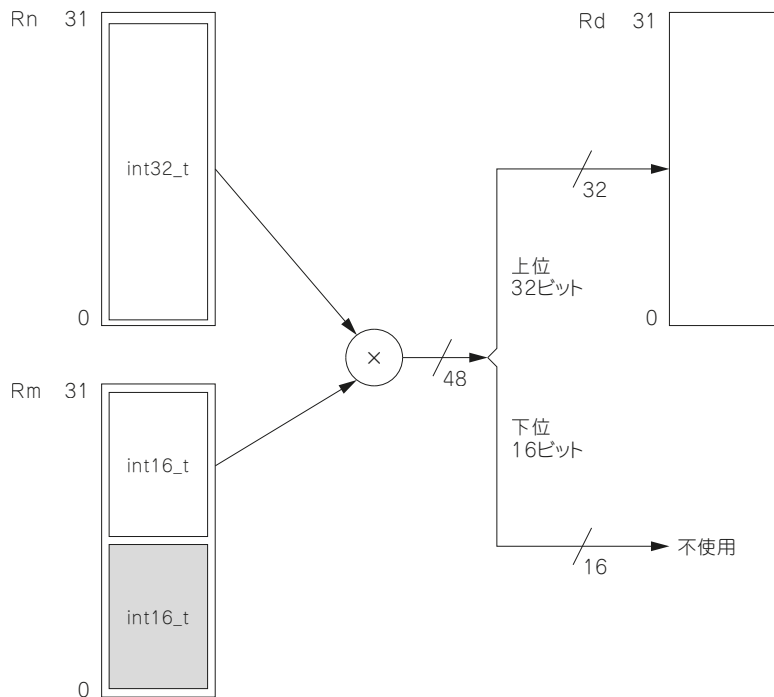
図B.39 SMLATT

SMULWB {<Rd>,<Rn>,<Rm>



図B.40 SMULWB

SMULWT {<Rd>,<Rn>,<Rm>



図B.41 SMULWT

SMLAWB <Rd>, <Rn>, <Rm>, <Ra>

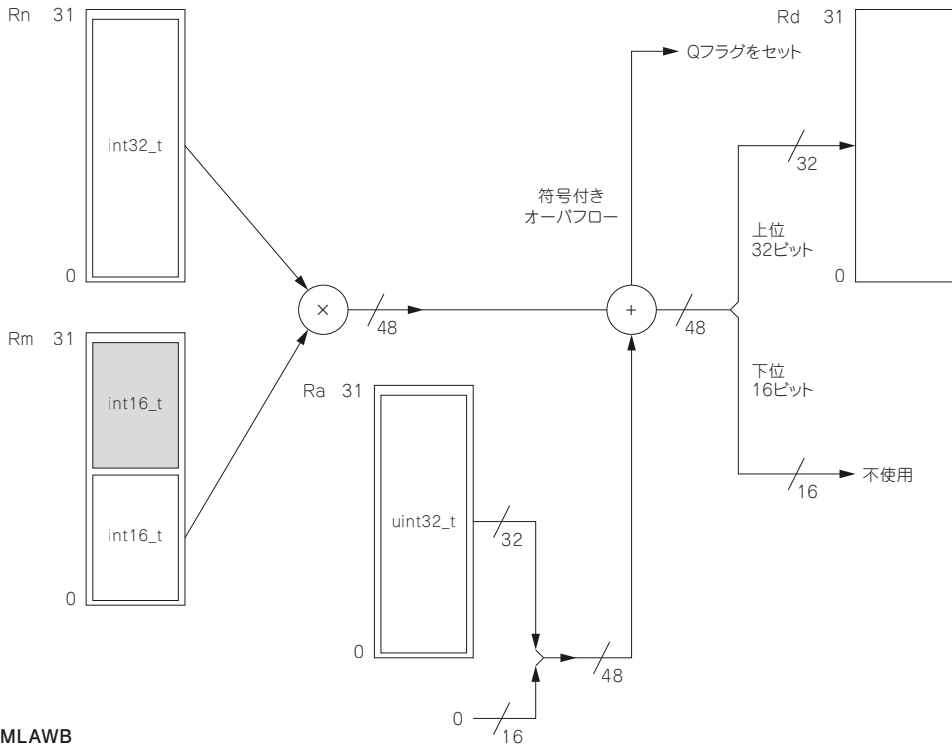


図 B.42 SMLAWB

SMLAWT <Rd>, <Rn>, <Rm>, <Ra>

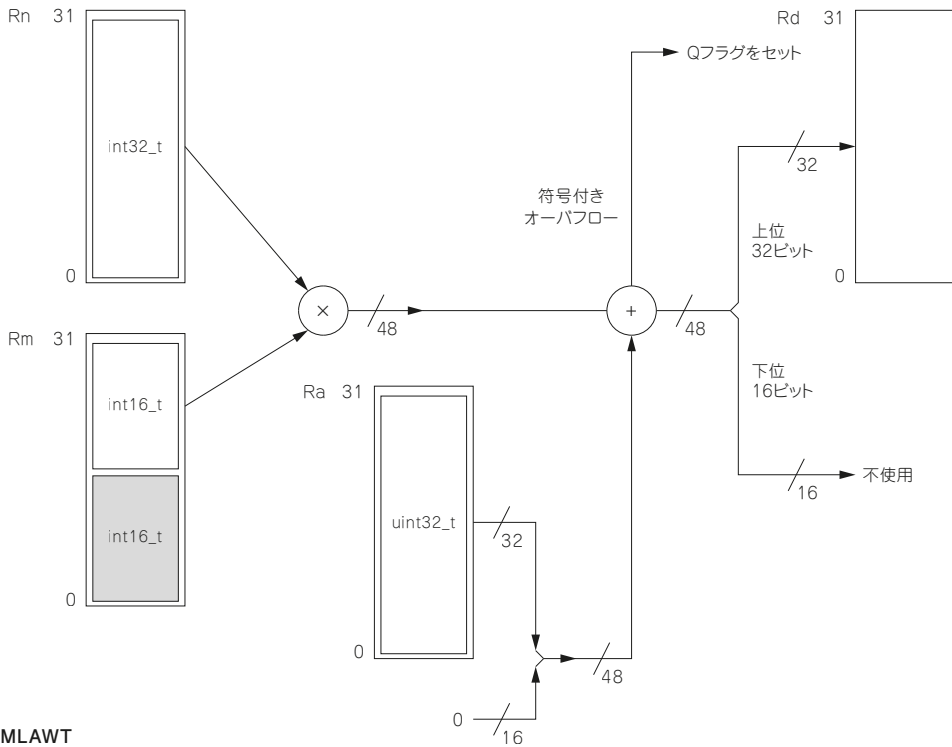
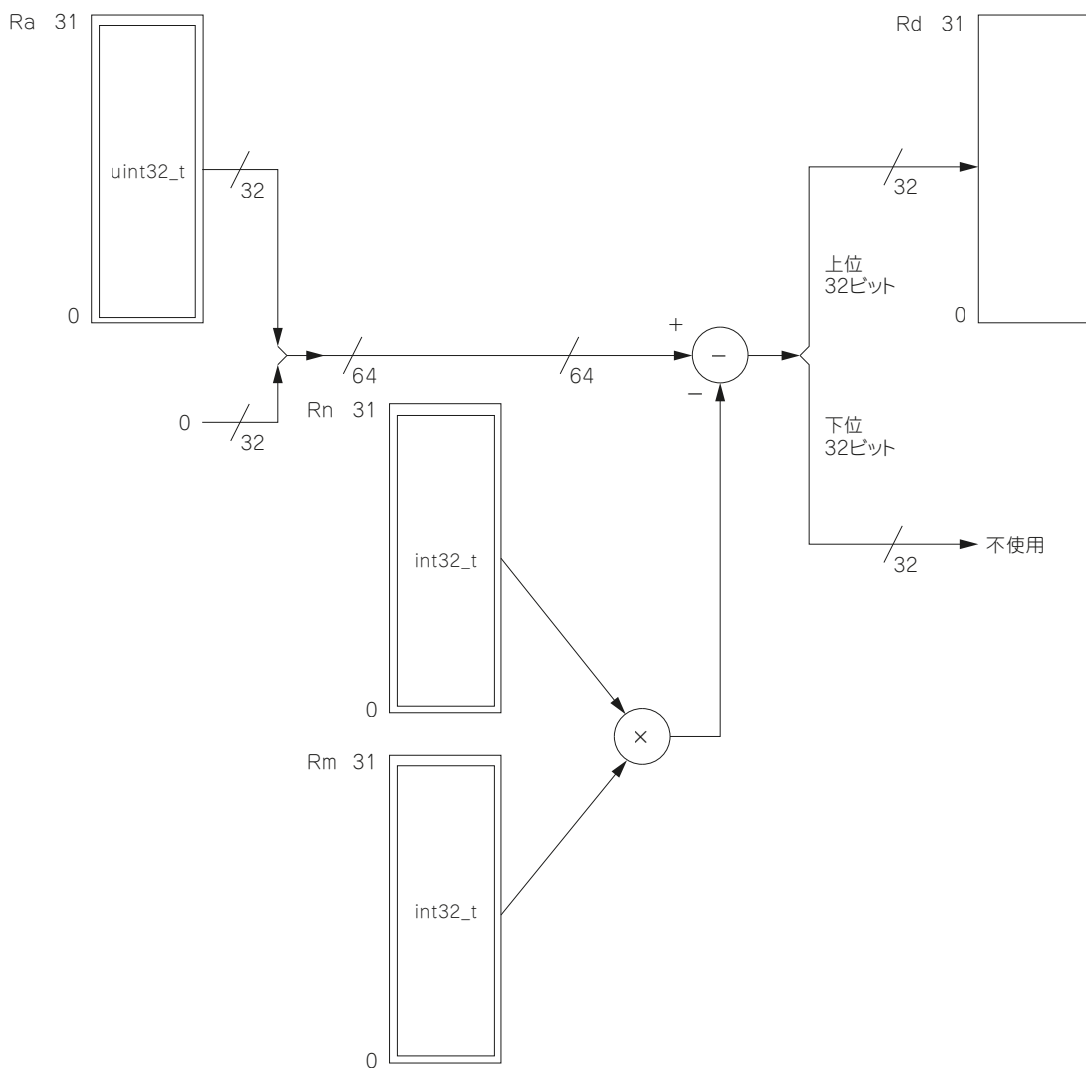


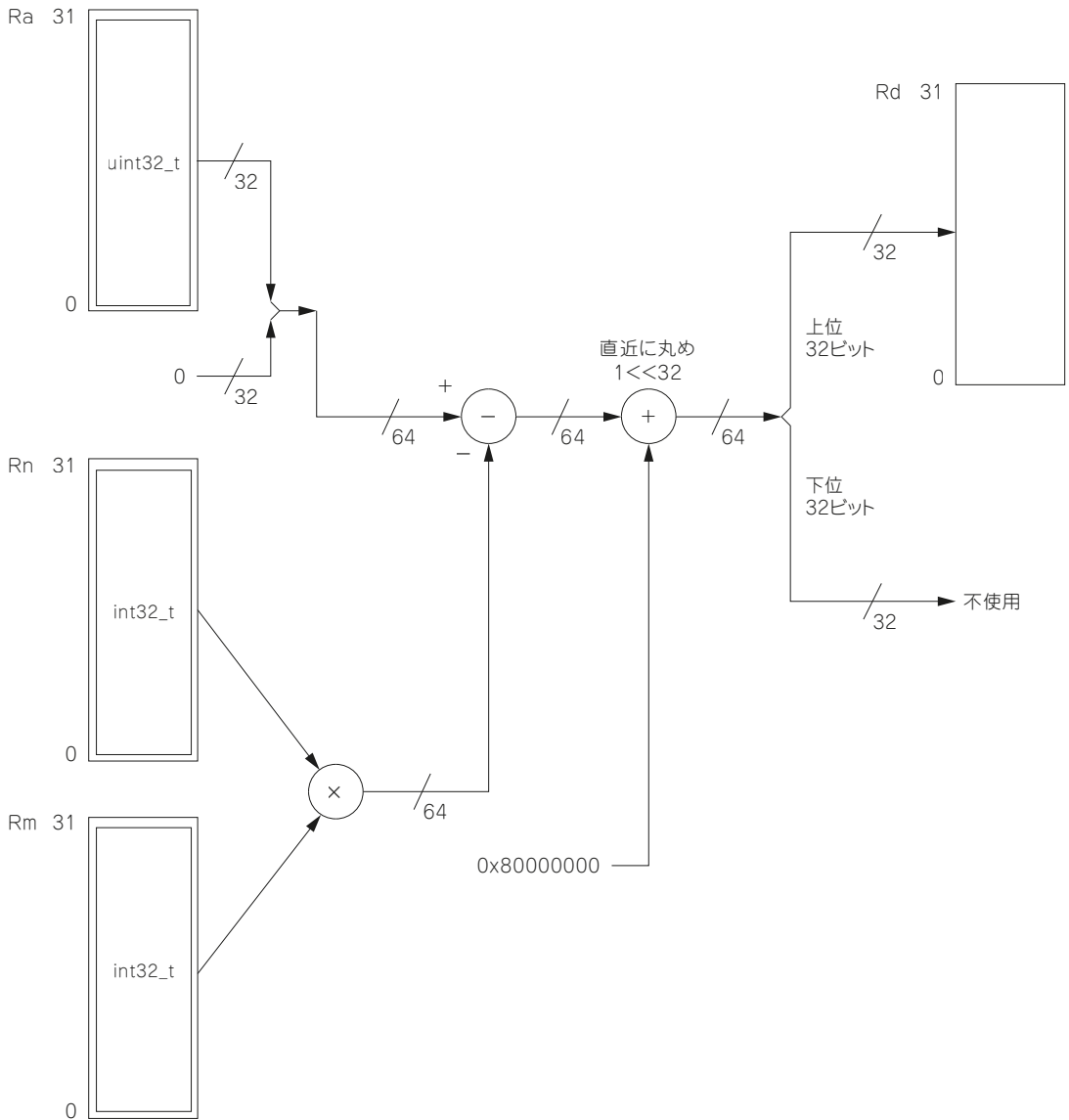
図 B.43 SMLAWT

SMMLS <Rd>, <Rn>, <Rm>, <Ra>



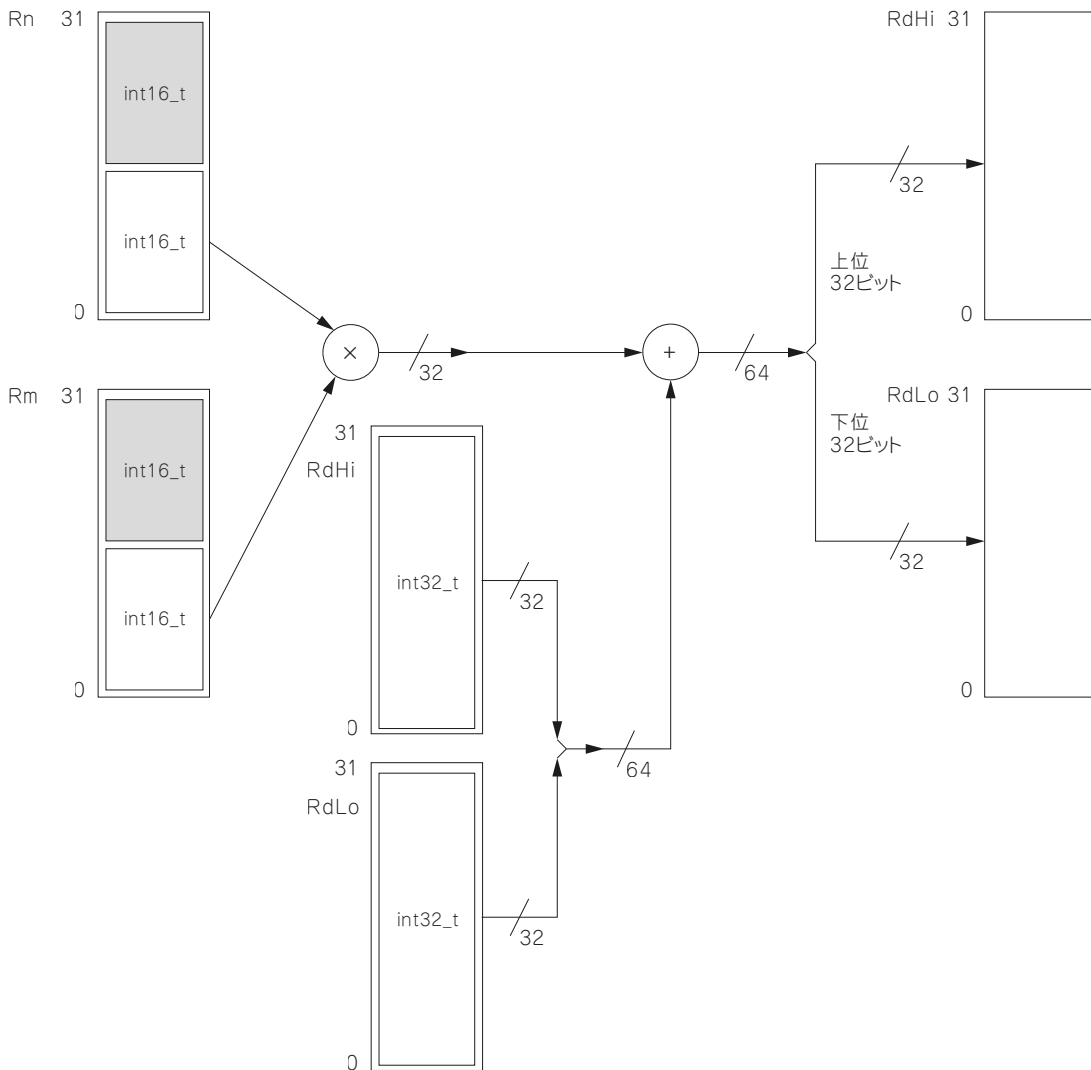
図B.44 SMMLS

SMMLSR <Rd>, <Rn>, <Rm>, <Ra>



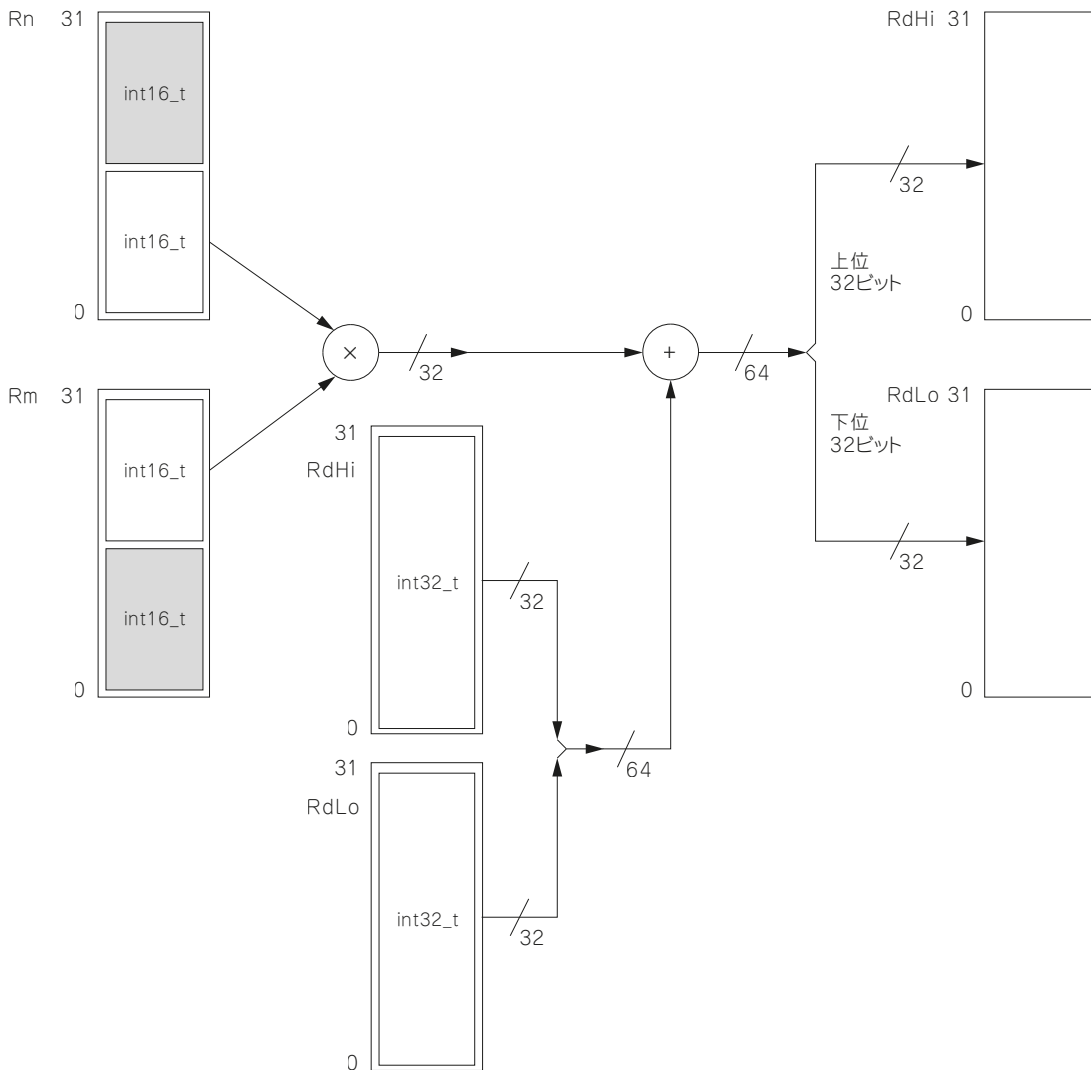
図B.45 SMMLSR

SMLALBB <RdLo>, <RdHi>, <Rn>, <Rm>



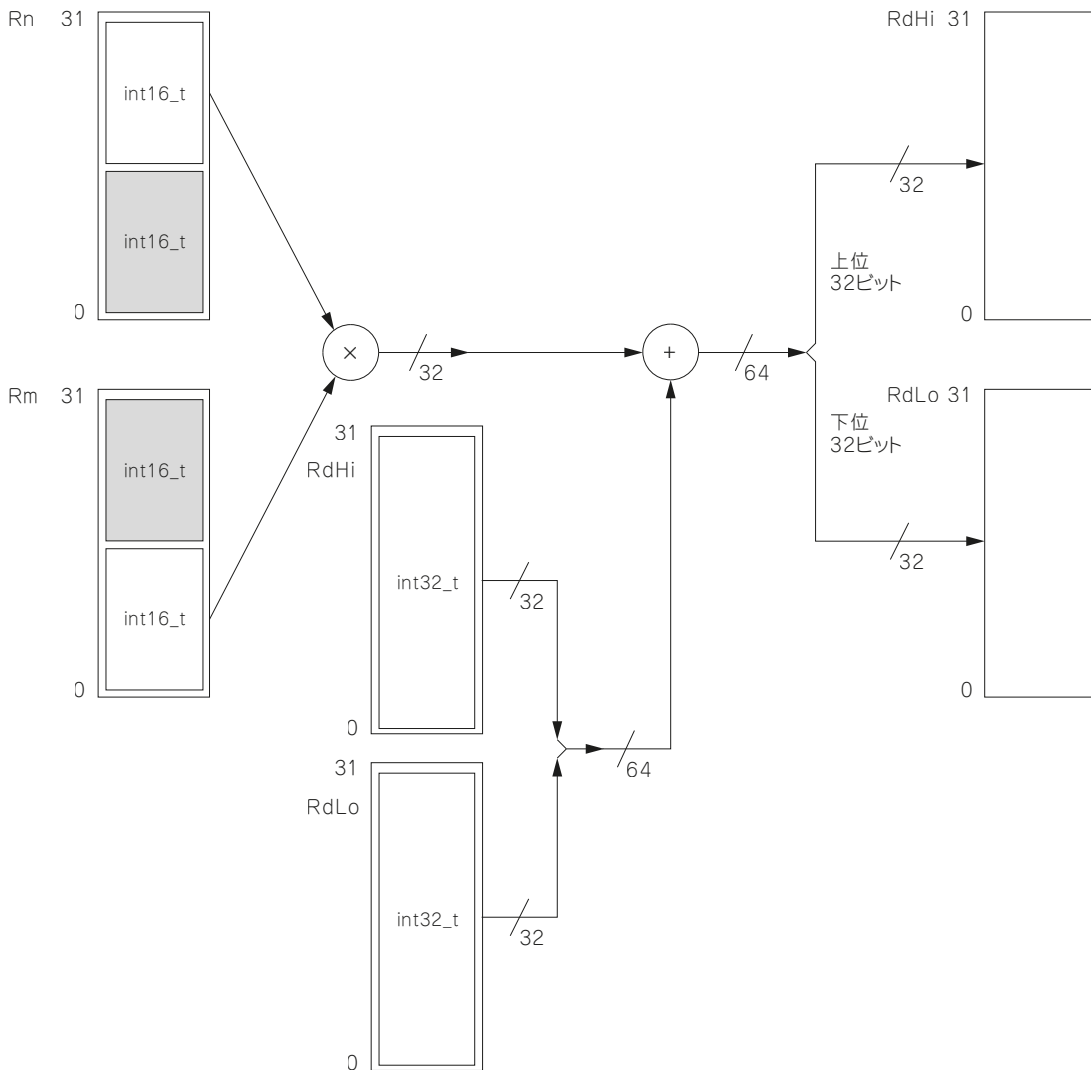
図B.46 SMLALBB

SMLALBT <RdLo>, <RdHi>, <Rn>, <Rm>



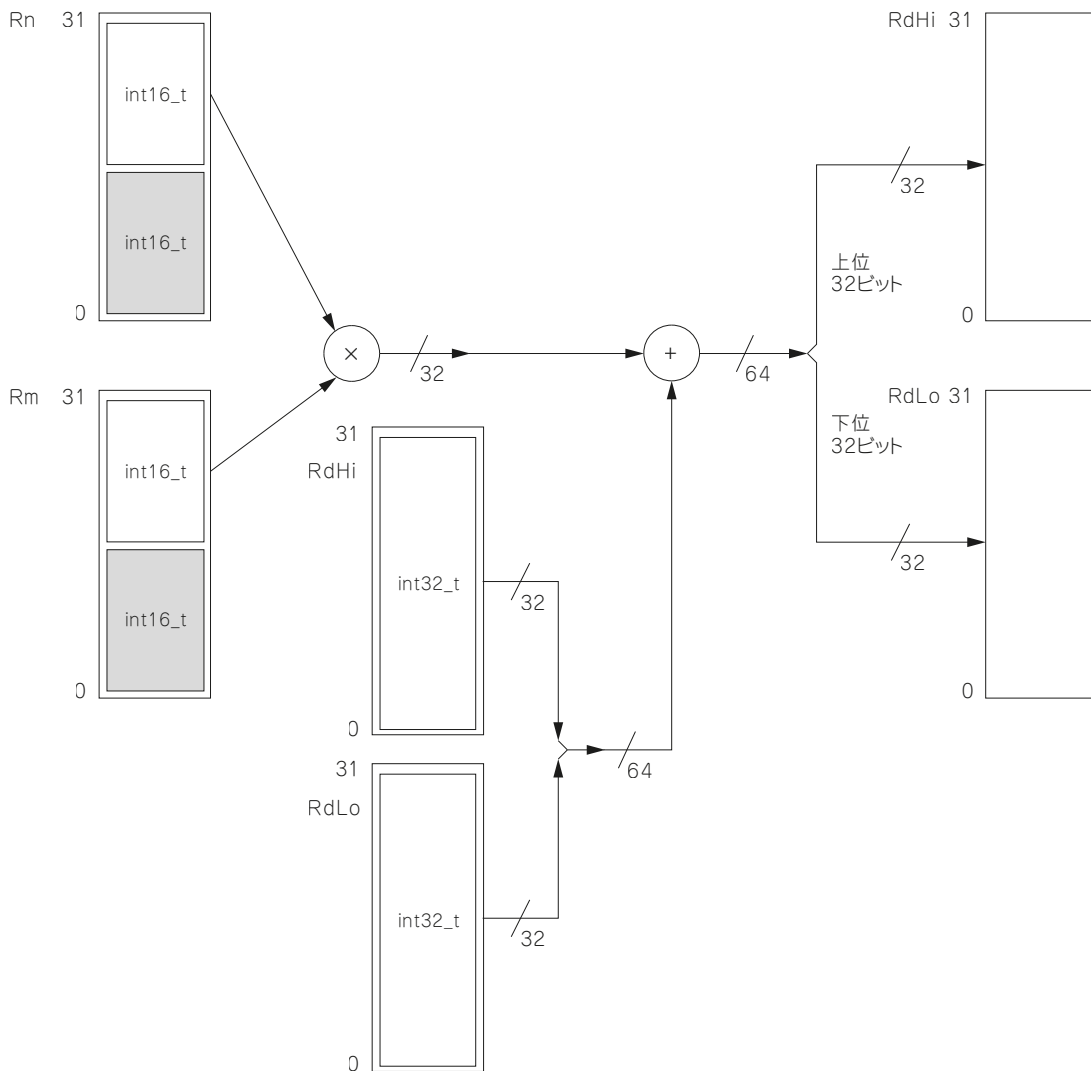
図B.47 SMLALBT

SMLALTB <RdLo>, <RdHi>, <Rn>, <Rm>



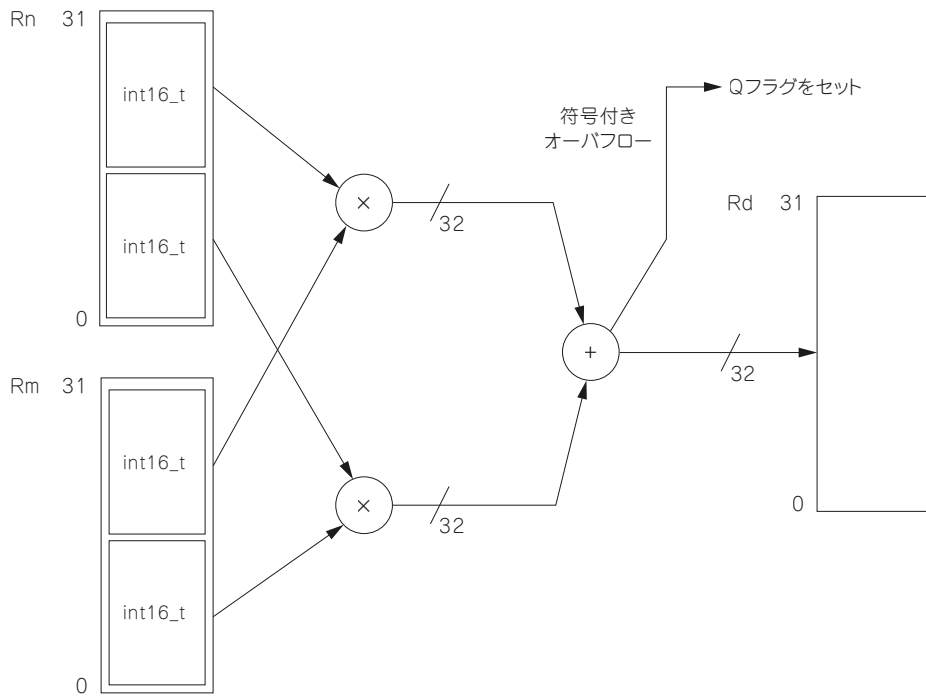
図B.48 SMLALTB

SMLALTT <RdLo>, <RdHi>, <Rn>, <Rm>



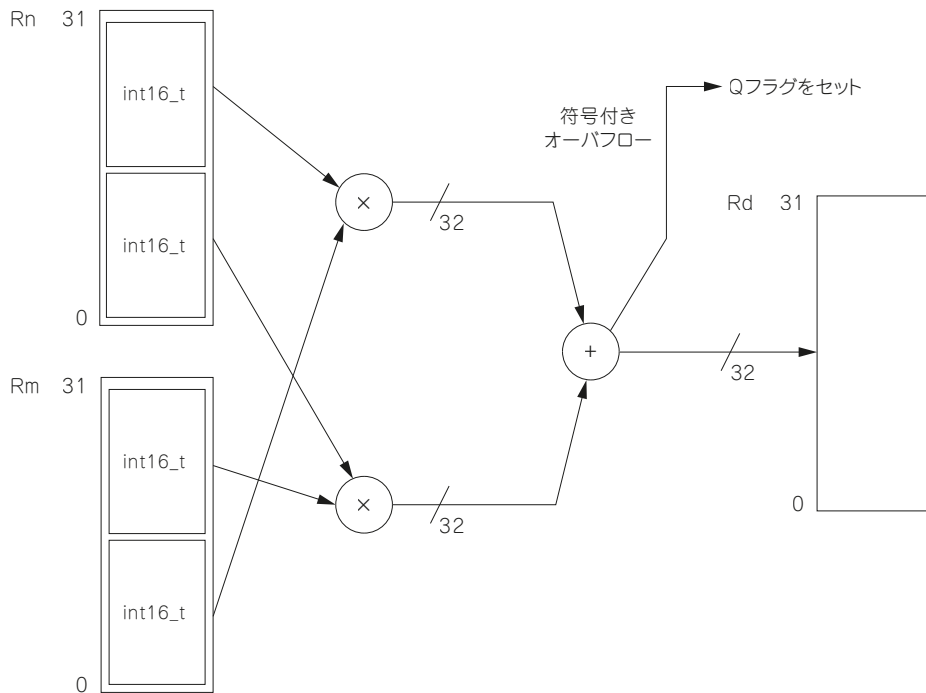
図B.49 SMLALTT

SMUAD {<Rd>,} <Rn>, <Rm>



図B.50 SMUAD

SMUADX {<Rd>,} <Rn>, <Rm>



図B.51 SMUADX

SMLAD <Rd>, <Rn>, <Rm>, <Ra>

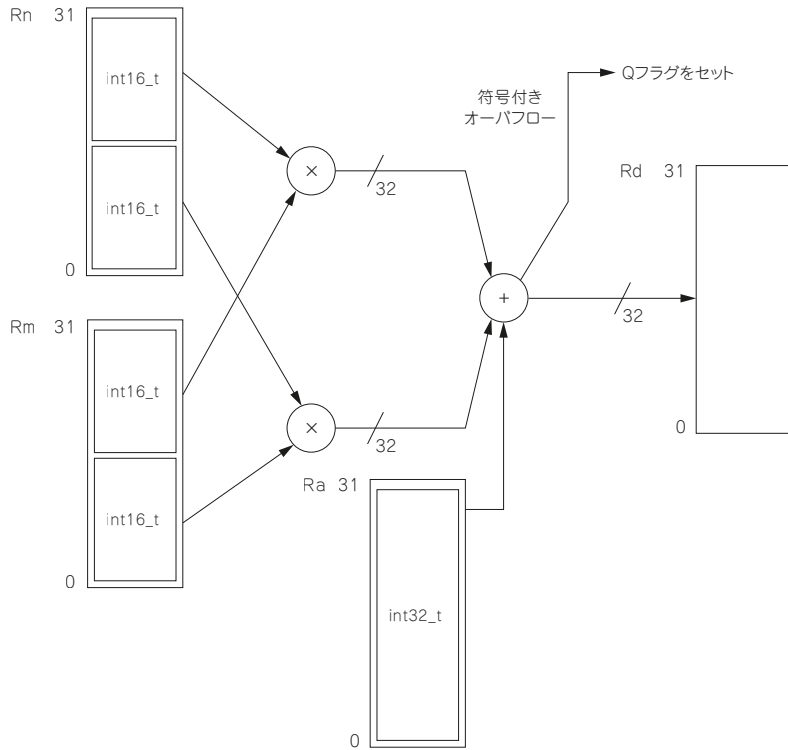


図 B.52 SMLAD

SMLADX <Rd>, <Rn>, <Rm>, <Ra>

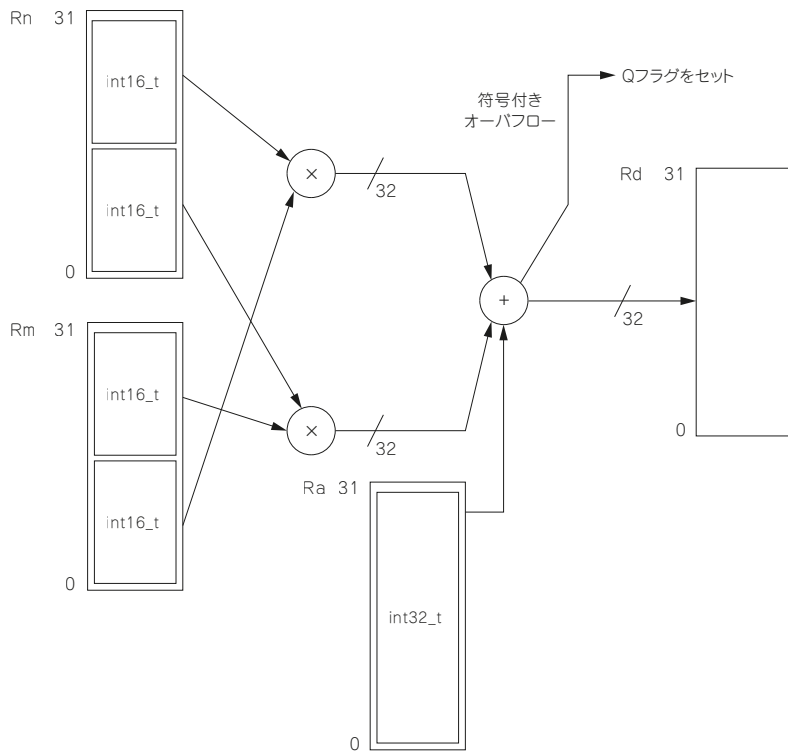
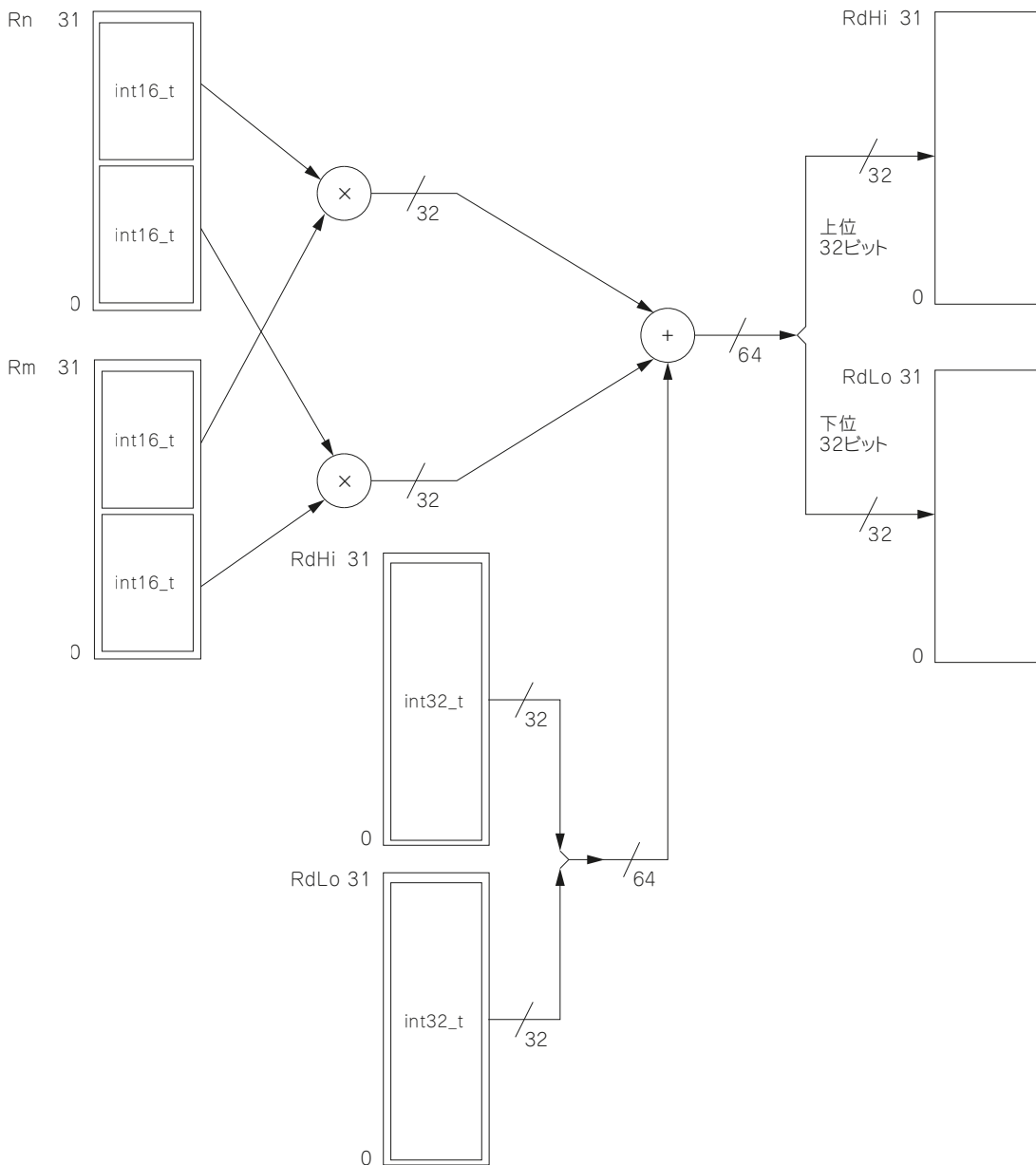


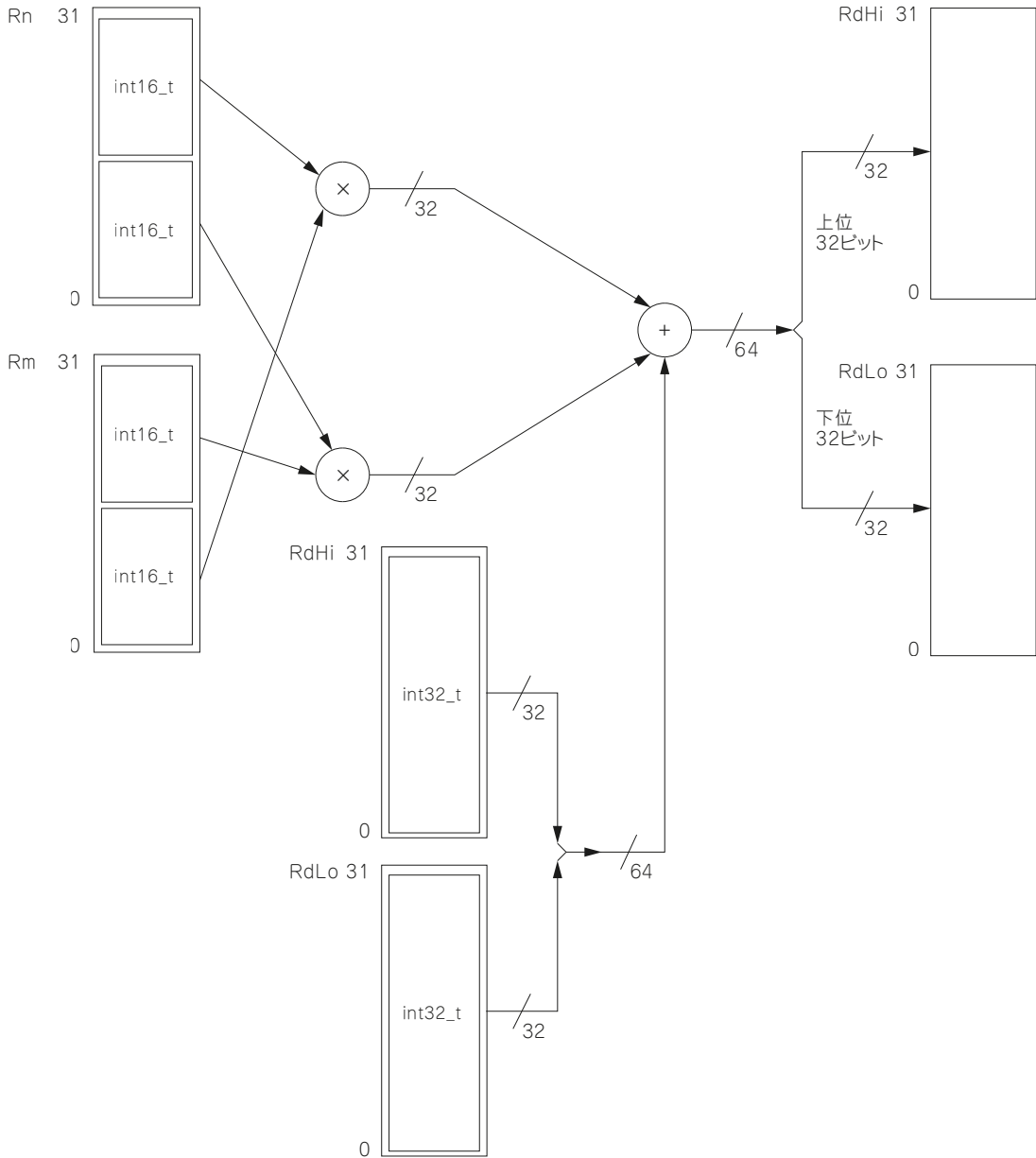
図 B.53 SMLADX

SMLALD <RdLo>, <RdHi>, <Rn>, <Rm>



図B.54 SMLALD

SMLALDX <RdLo>, <RdHi>, <Rn>, <Rm>



図B.55 SMLALDX

SMUSD (<Rd>,) <Rn>, <Rm>

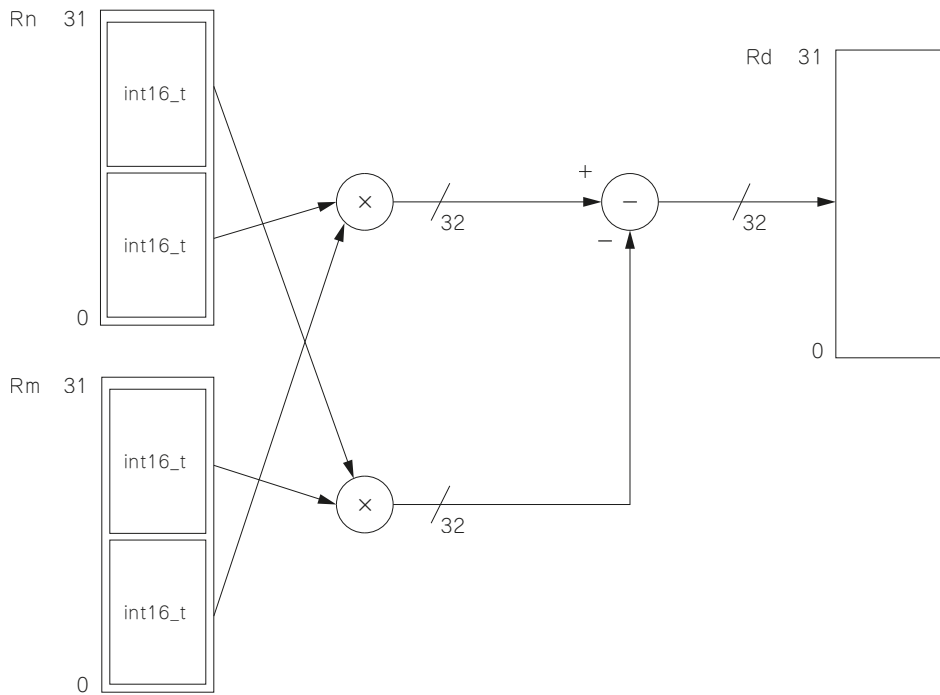


図 B.56 SMUSD

SMUSDX (<Rd>,) <Rn>, <Rm>

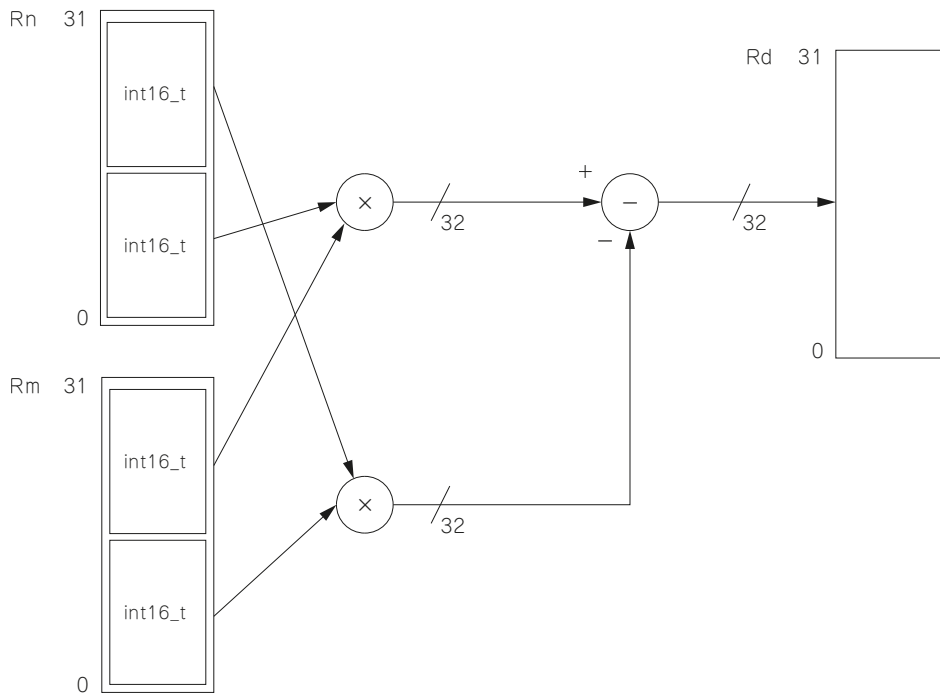
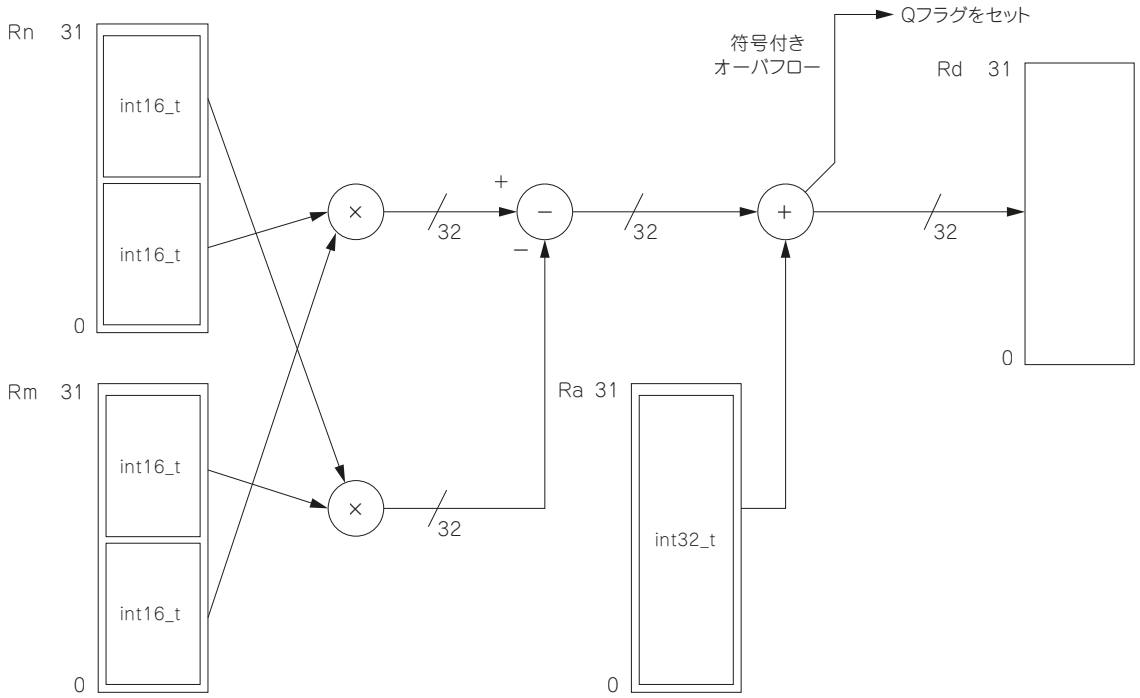


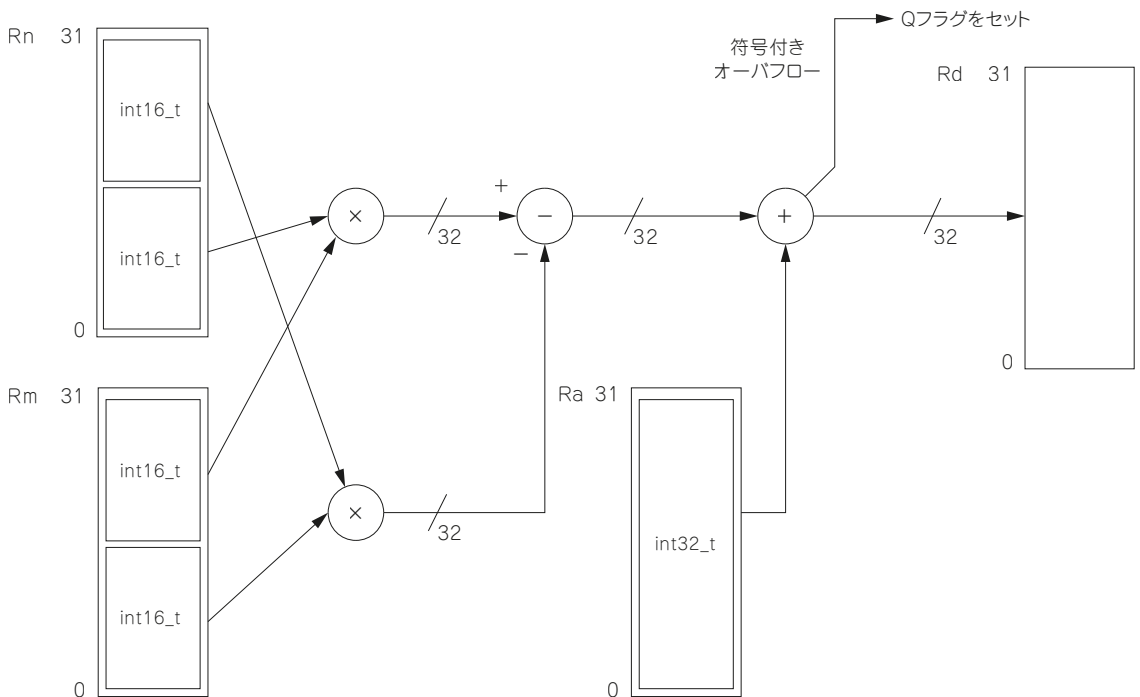
図 B.57 SMUSDX

SMLSDD <Rd>, <Rn>, <Rm>, <Ra>



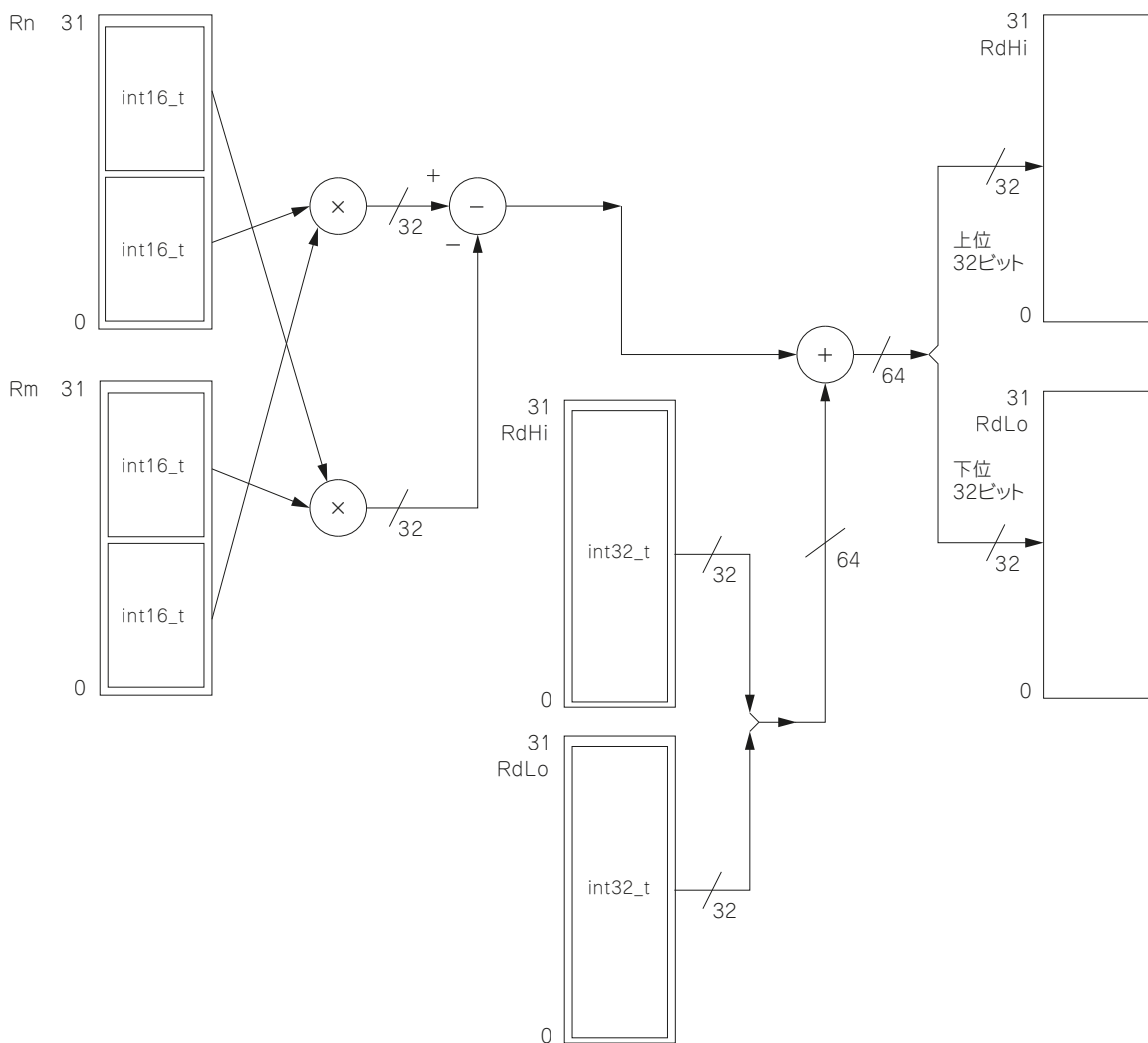
図B.58 SMLSDD

SMLSDDX <Rd>, <Rn>, <Rm>, <Ra>



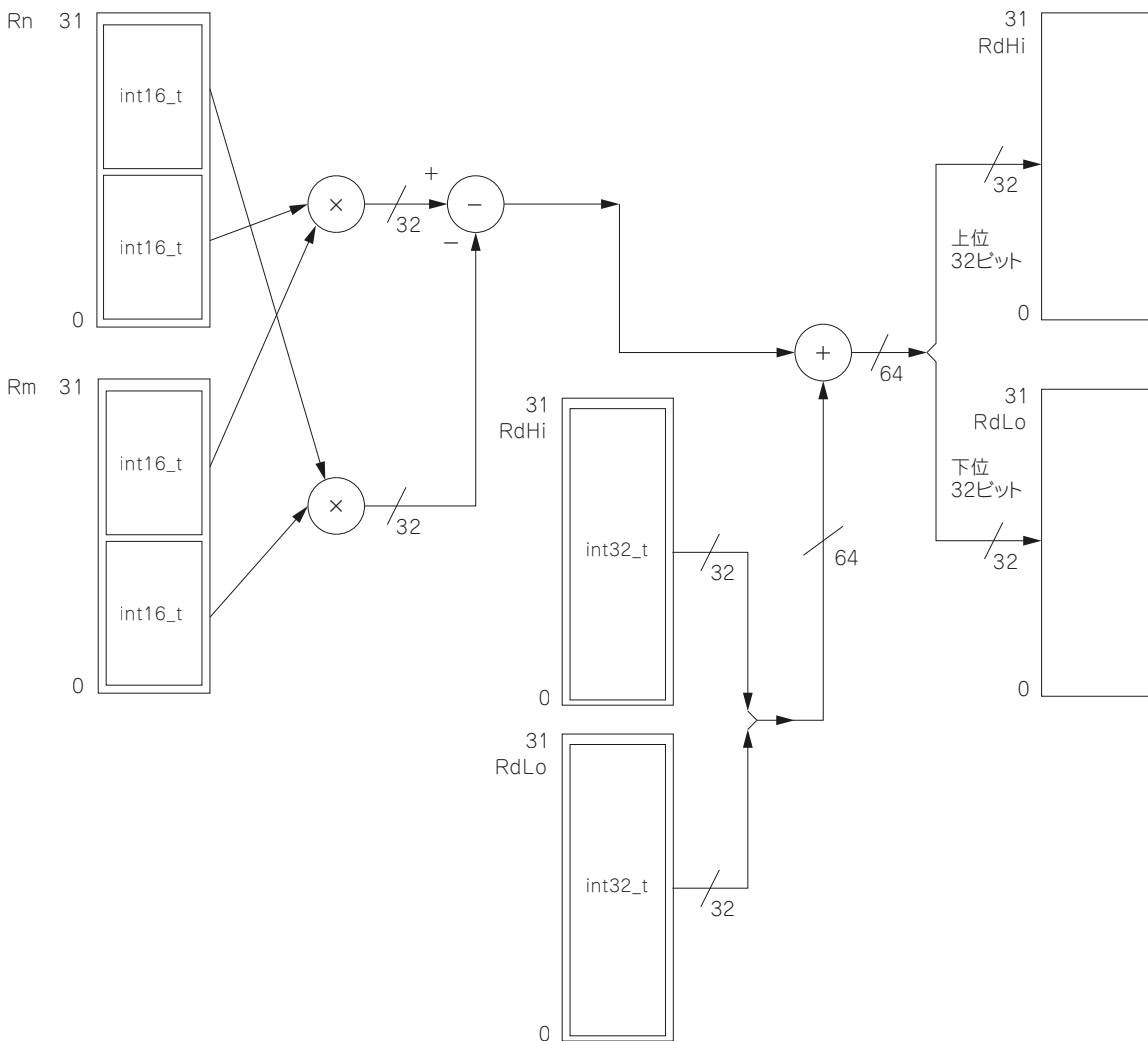
図B.59 SMLSDDX

SMLS LD <RdLo>, <RdHi>, <Rn>, <Rm>

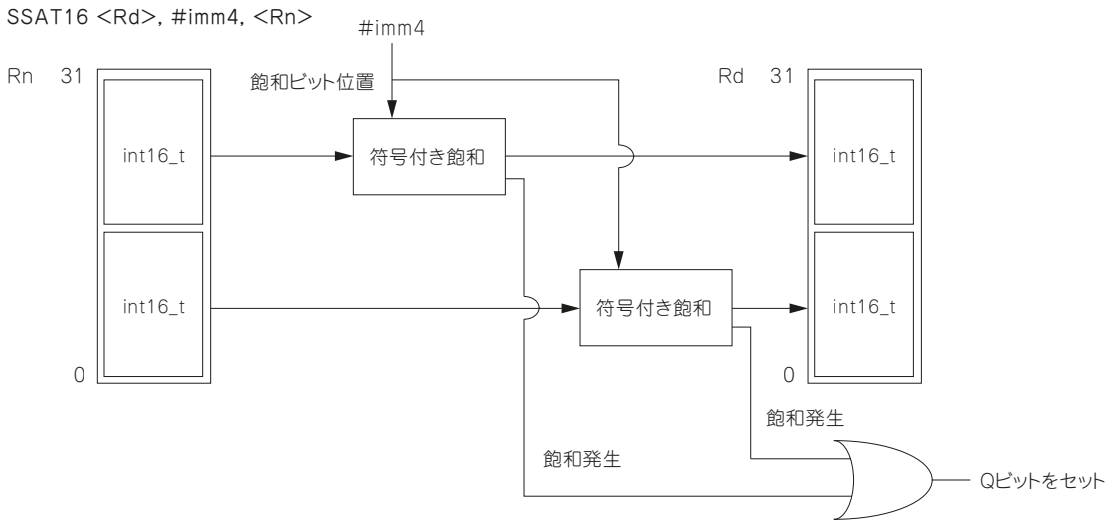


図B.60 SMLS LD

SMLSLDX <RdLo>, <RdHi>, <Rn>, <Rm>

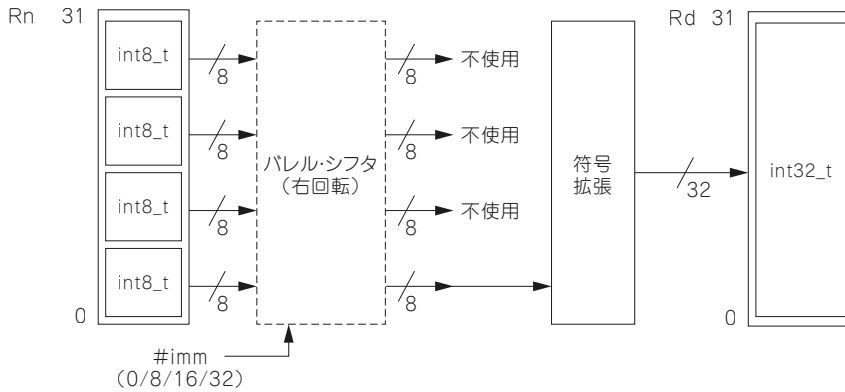


図B.61 SMLSLDX



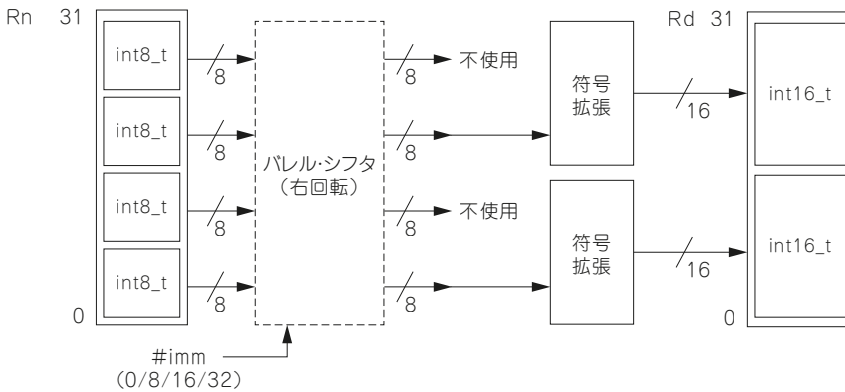
図B.62 SSAT16

SXTB {<Rd>,} <Rn> {, ROR #imm}  
 (DSP拡張が実装されていなくてもCortex-M33プロセッサでは利用可能)



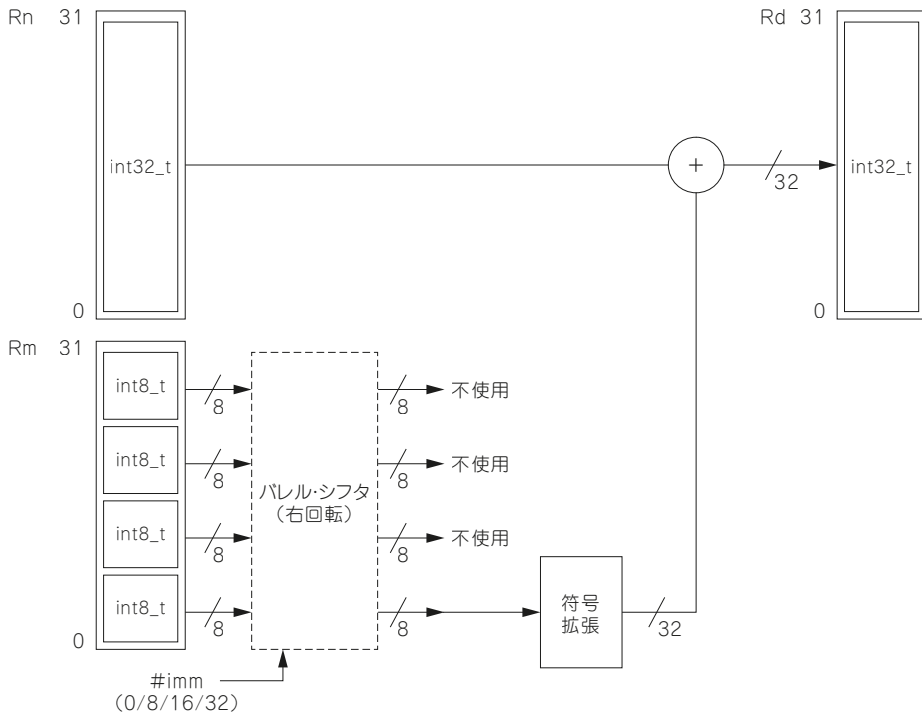
図B.63 SXTB

SXTB16 (<Rd>,) <Rn> {, ROR #imm}



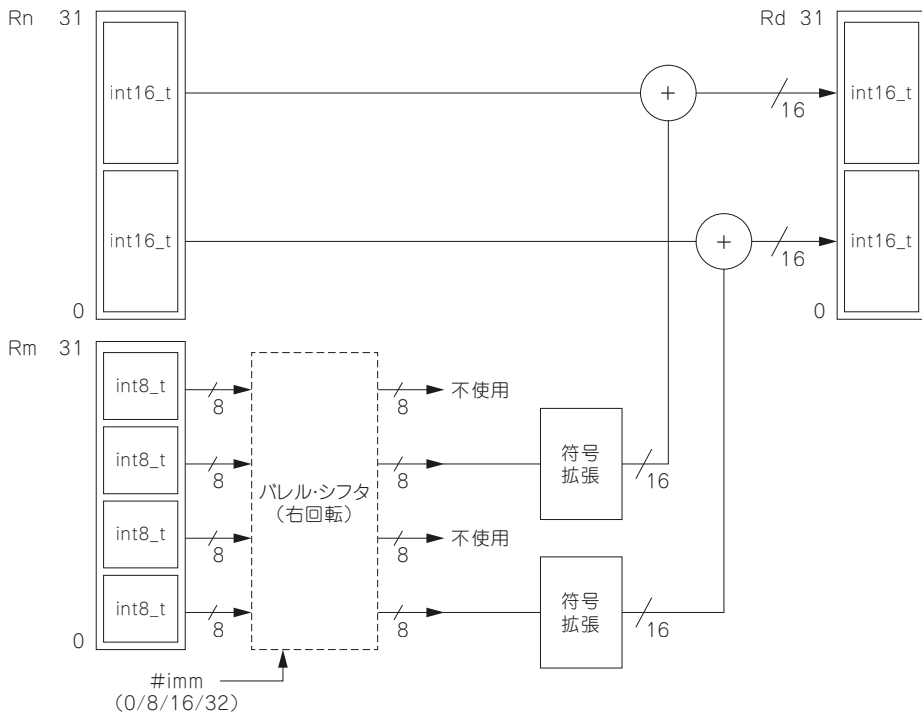
図B.64 SXTB16

SXTAB {<Rd>}, <Rn>, <Rm> {, ROR #imm}



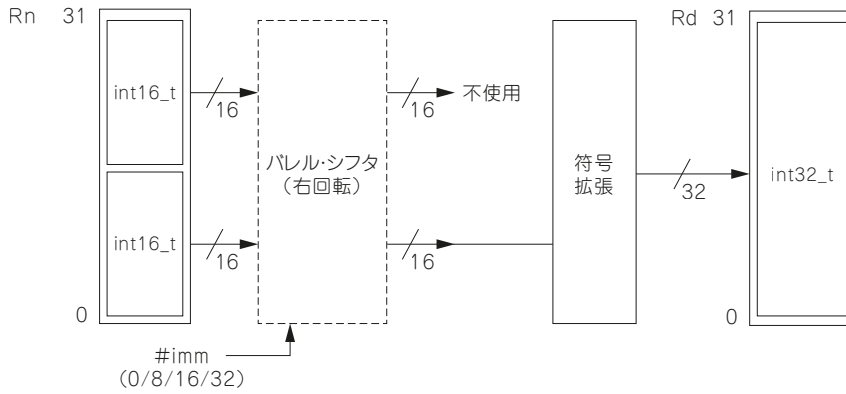
図B.65 SXTAB

SXTAB16 {<Rd>}, <Rn>, <Rm> {, ROR #imm}



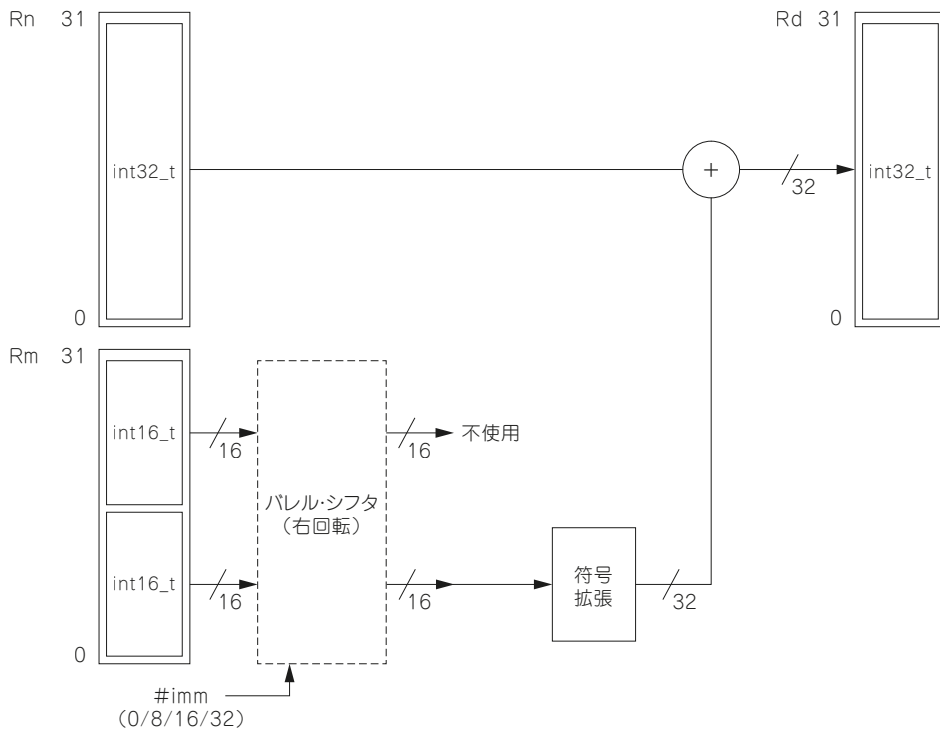
図B.66 SXTAB16

SXTH {<Rd>,} <Rn>, <Rm> {, ROR #imm}  
 (DSP拡張が実装されていなくてもCortex-M33プロセッサでは使用可能)



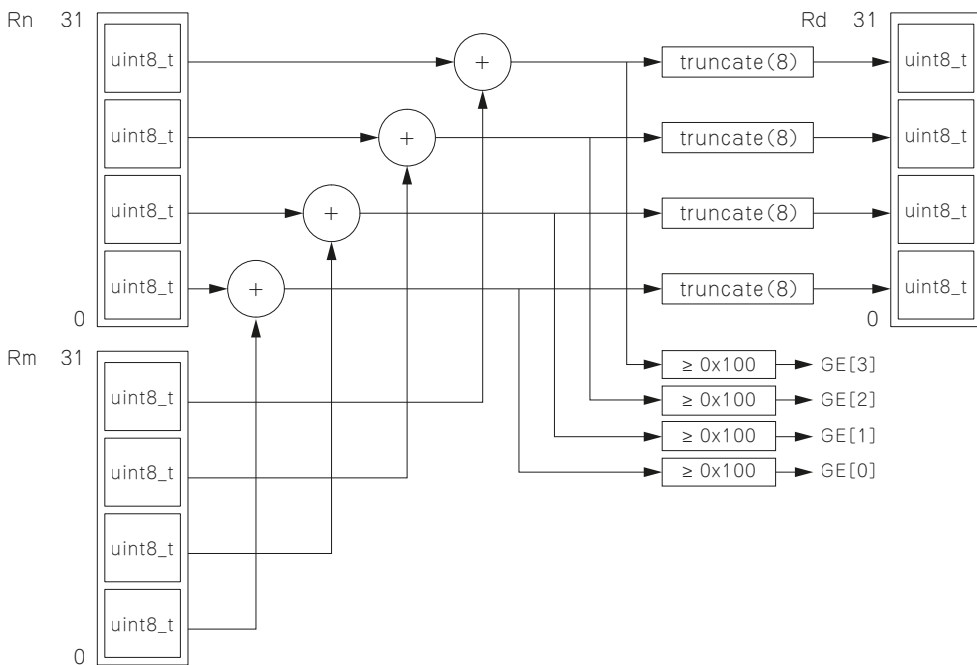
図B.67 SXTH

SXTAH {<Rd>,} <Rn>, <Rm> {, ROR #imm}



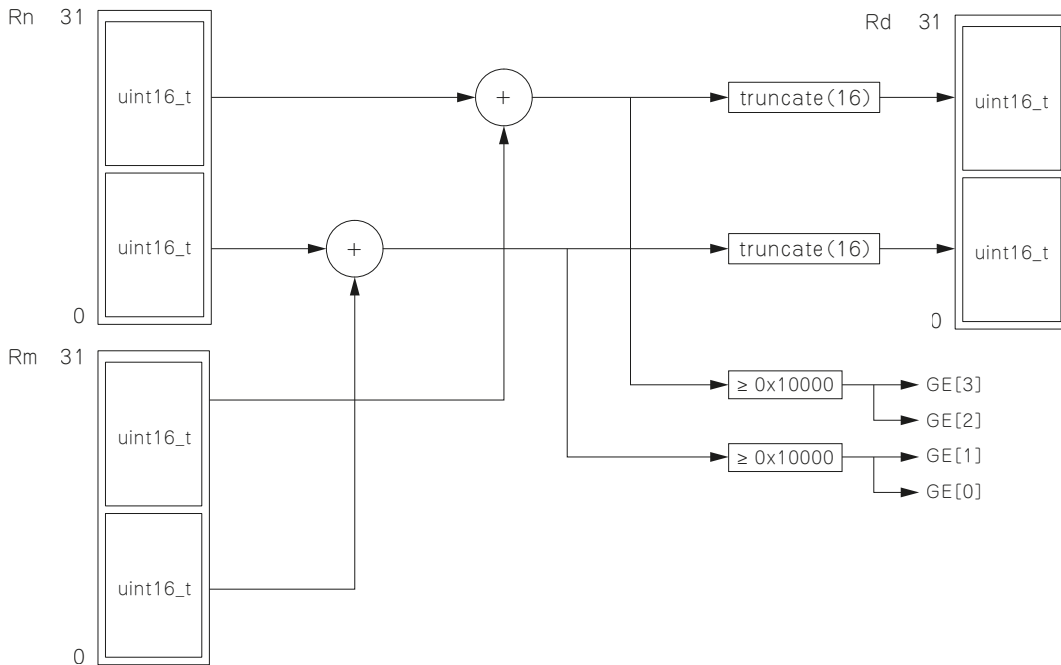
図B.68 SXTAH

UADD8 {<Rd>,} <Rn>, <Rm>



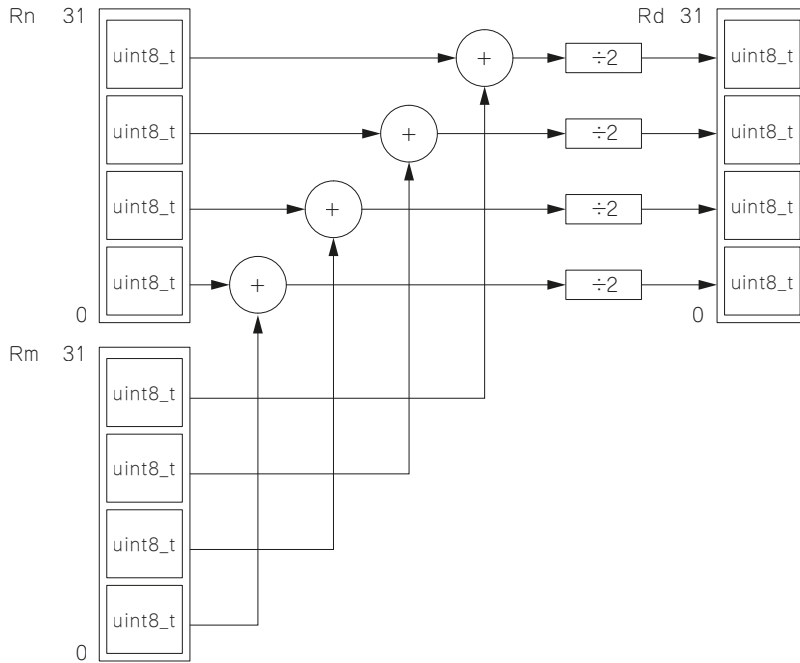
図B.69 UADD8

UADD16 {<Rd>,} <Rn>, <Rm>



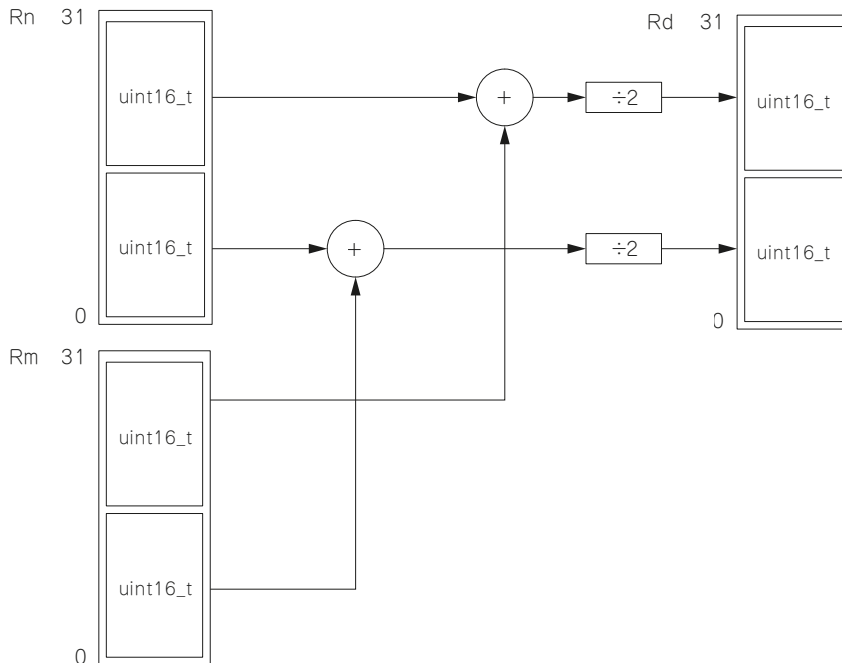
図B.70 UADD16

UHADD8 (<Rd>,) <Rn>, <Rm>



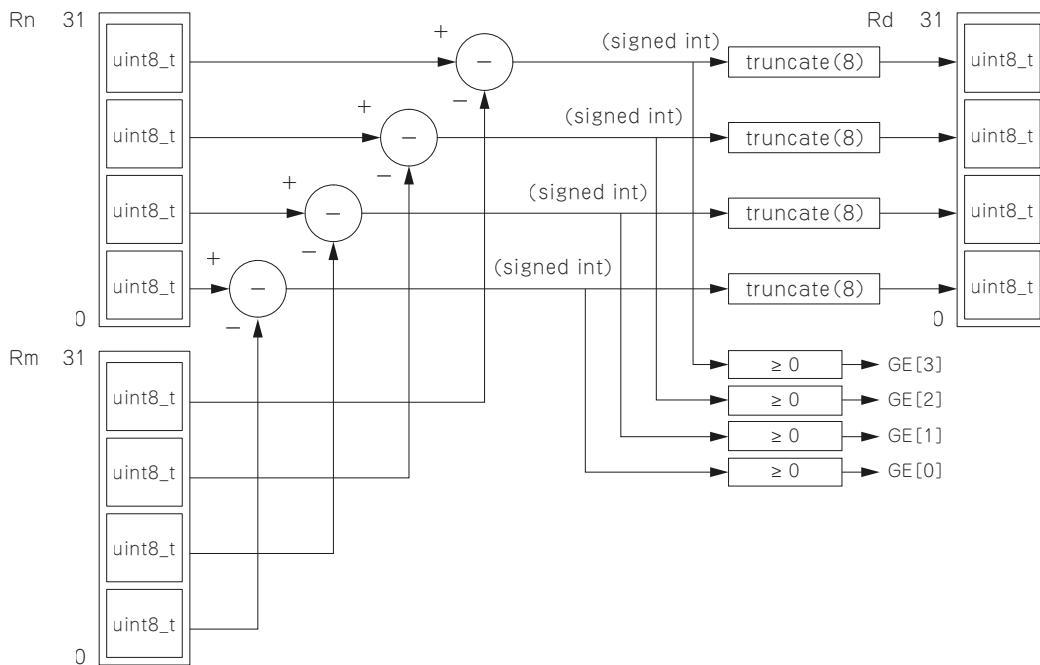
図B.71 UHADD8

UHADD16 {<Rd>,) <Rn>, <Rm>



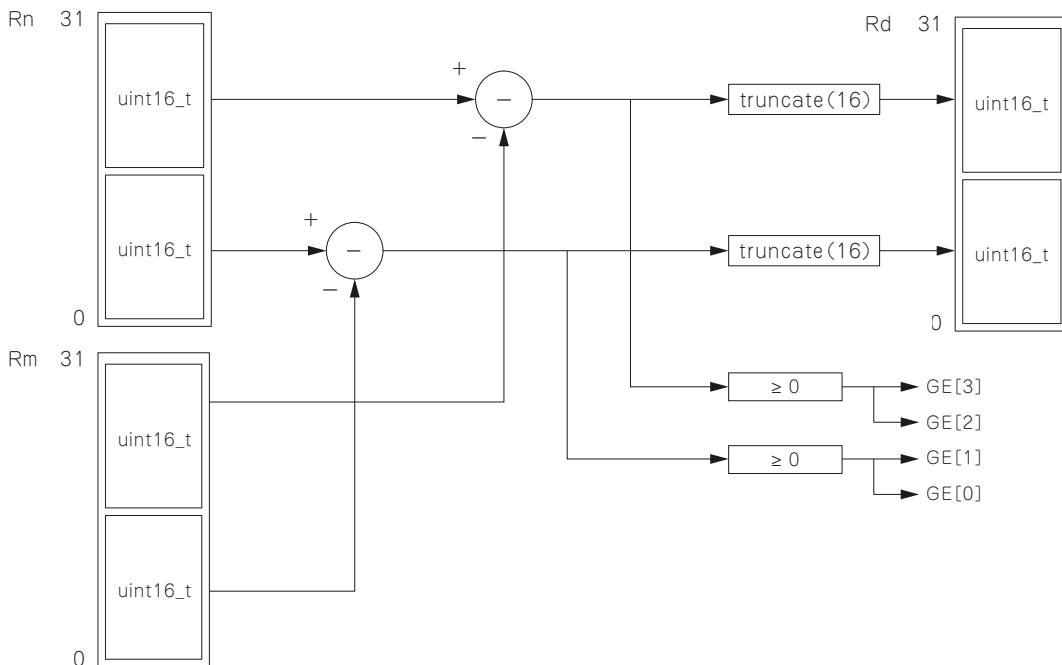
図B.72 UHADD16

USUB8 {<Rd>,} <Rn>, <Rm>



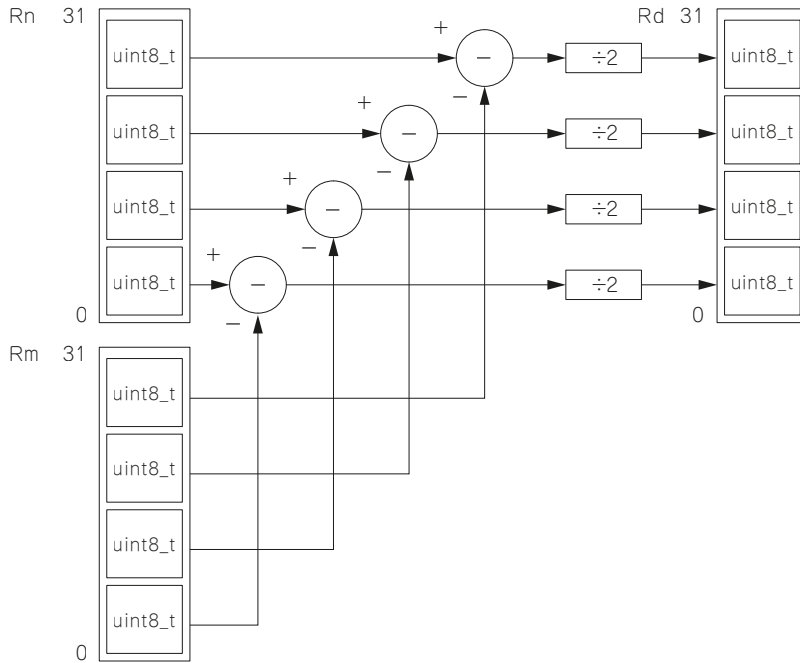
図B.73 USUB8

USUB16 {<Rd>,} <Rn>, <Rm>



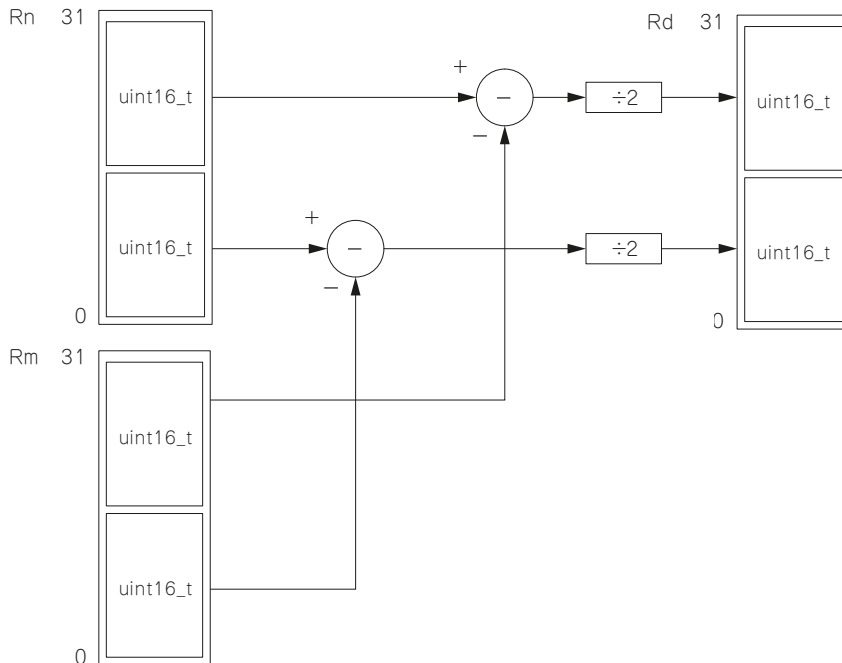
図B.74 USUB16

UHSUB8 (<Rd>,) <Rn>, <Rm>



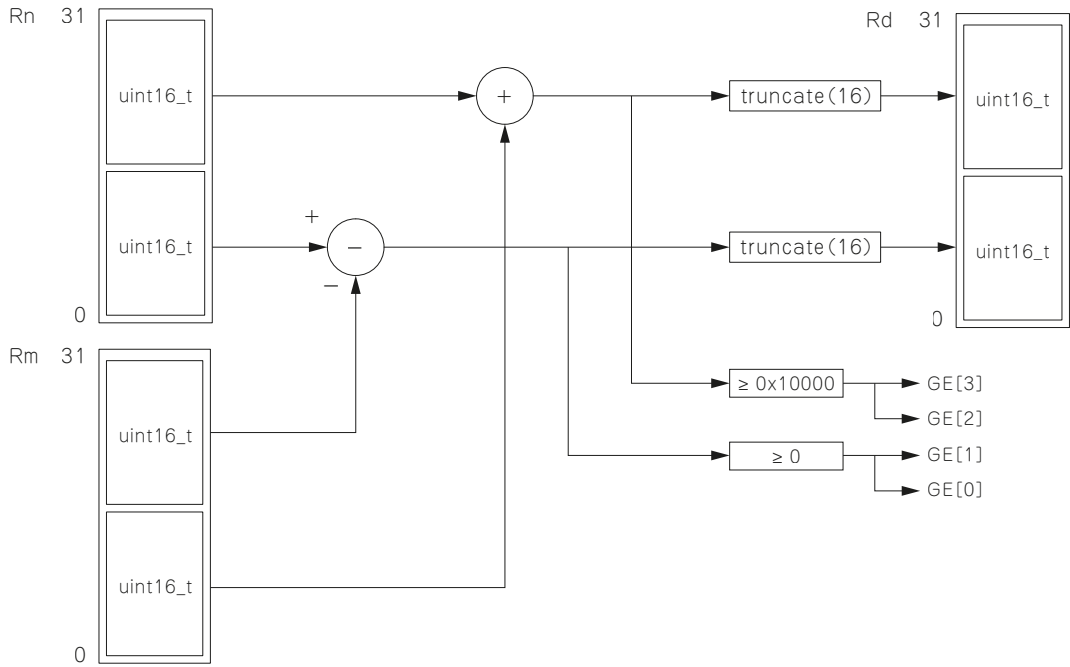
図B.75 UHSUB8

UHSUB16 (<Rd>,) <Rn>, <Rm>



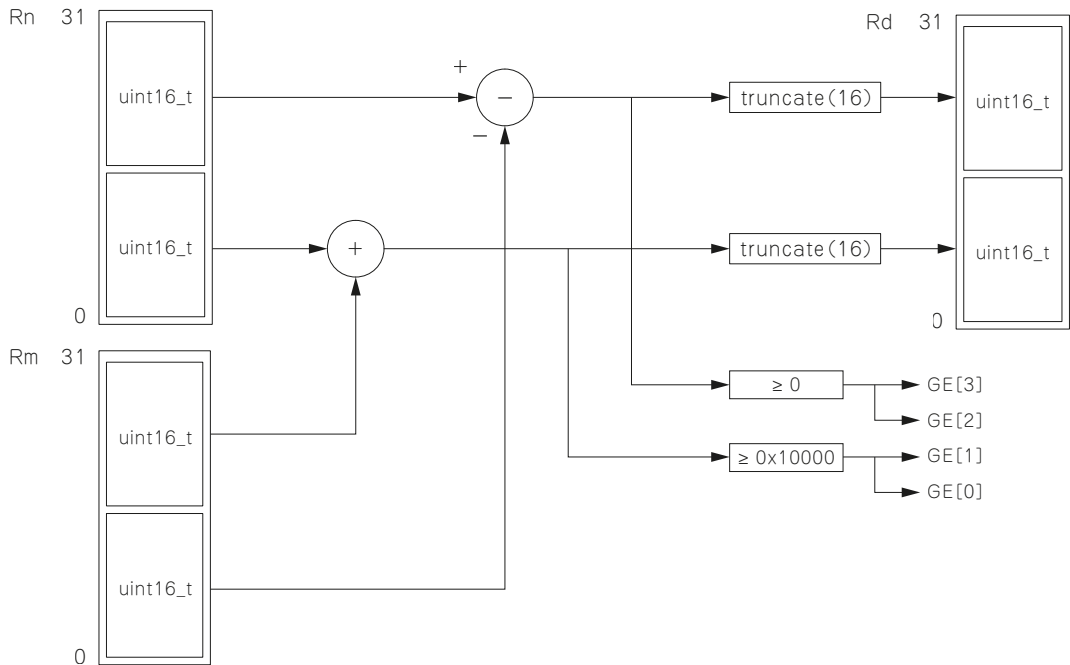
図B.76 UHSUB16

UASX (<Rd>,) <Rn>, <Rm>



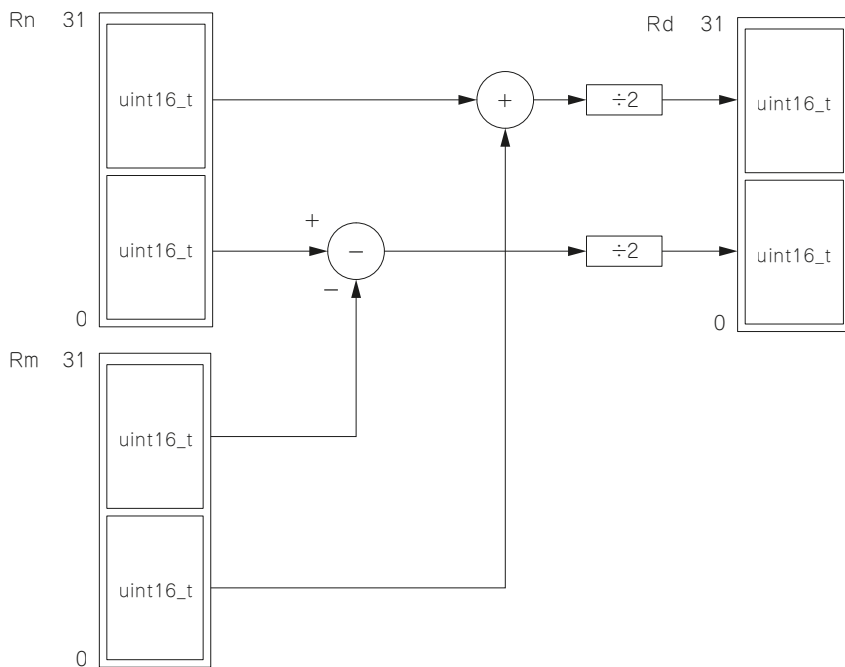
図B.77 UASX

USAX (<Rd>,) <Rn>, <Rm>



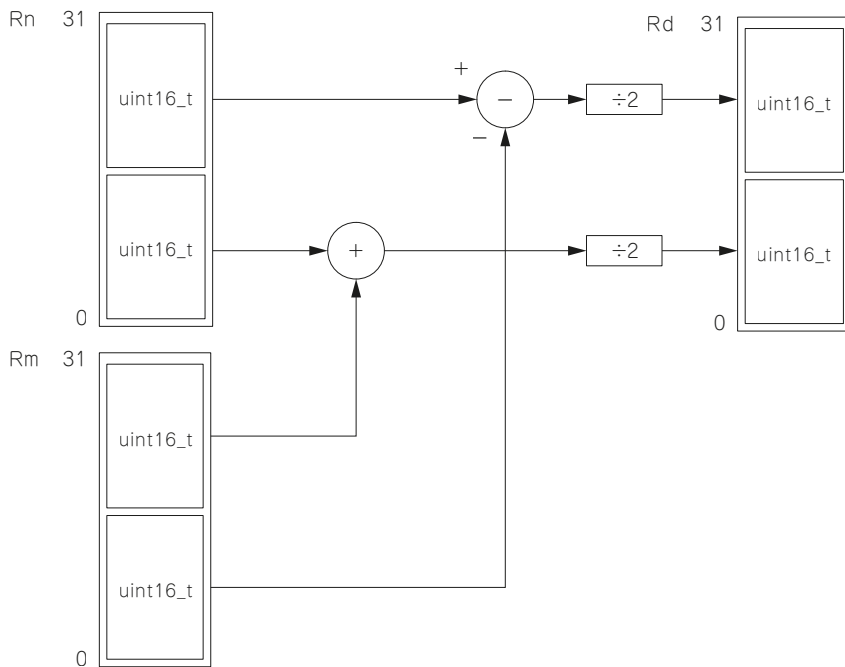
図B.78 USAX

UHASX {<Rd>,<Rn>, <Rm>



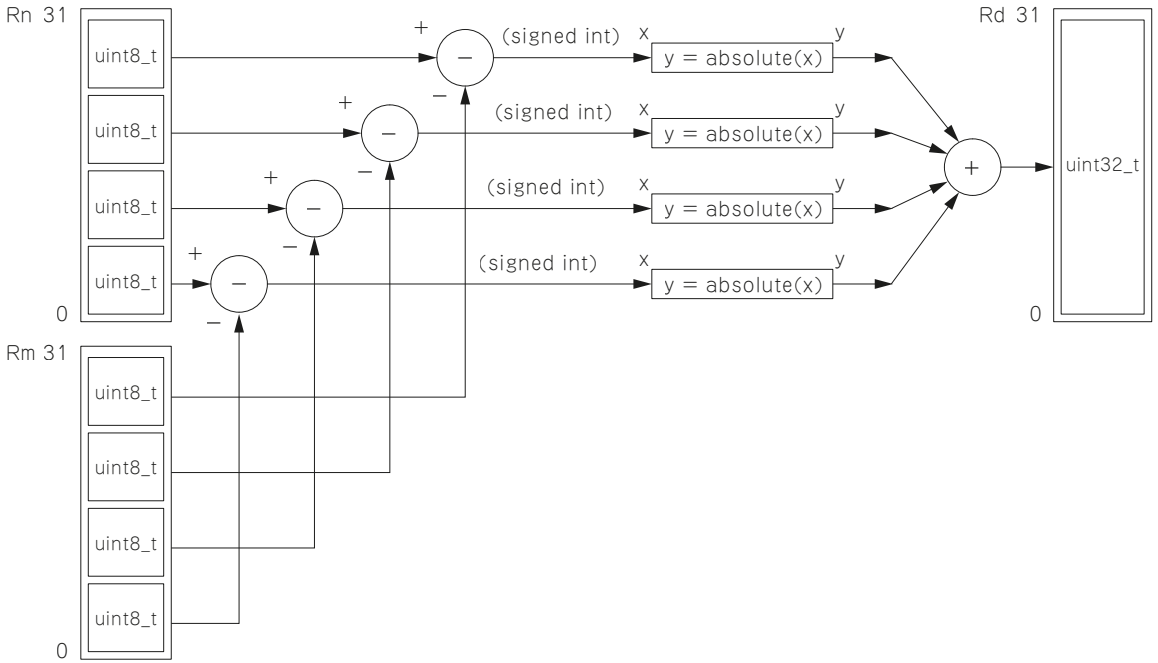
図B.79 UHASX

UHSAX {<Rd>,<Rn>, <Rm>



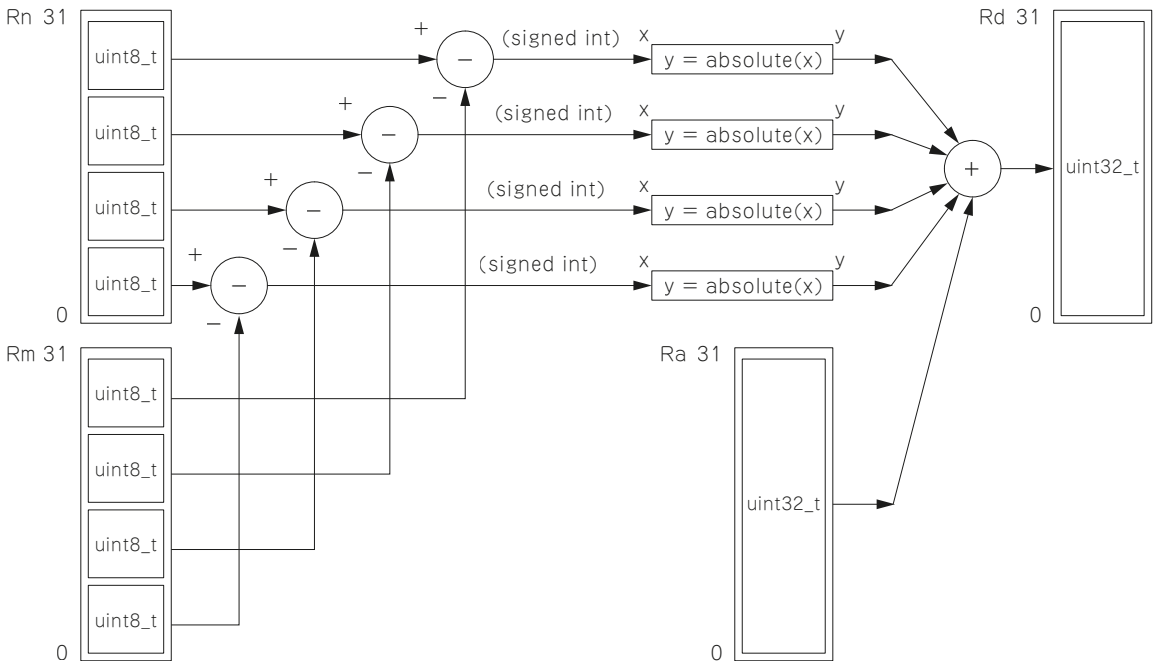
図B.80 UHSAX

USAD8 (<Rd>, <Rn>, <Rm>)

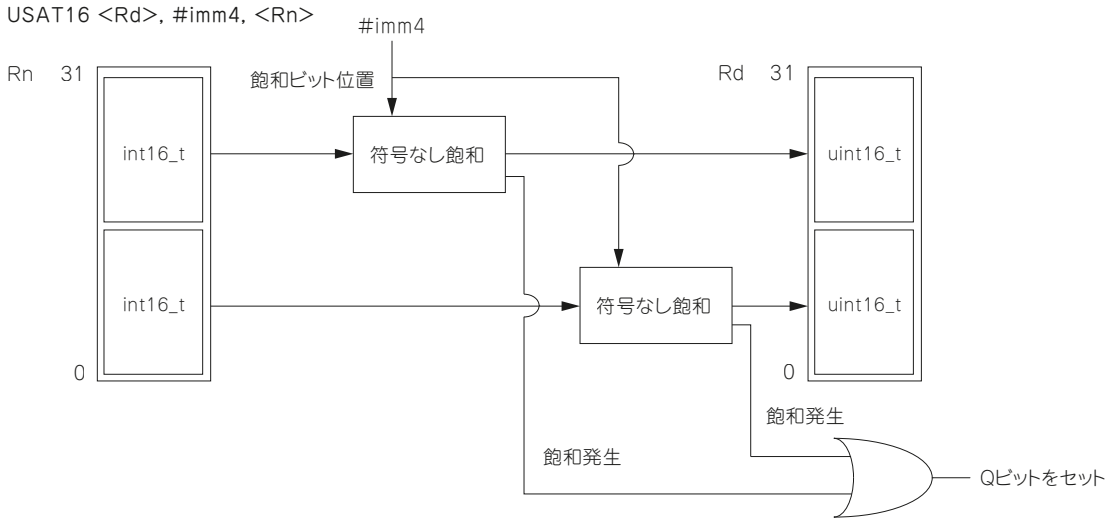


図B.81 USAD8

USADA8 (<Rd>, <Rn>, <Rm>)

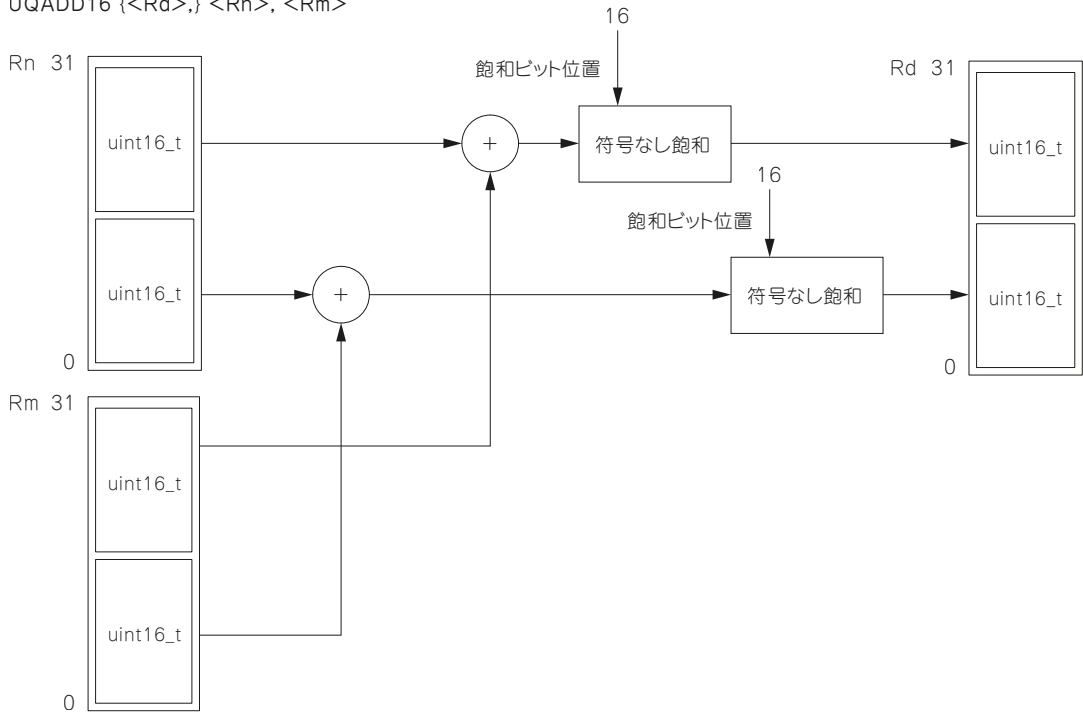


図B.82 USADA8



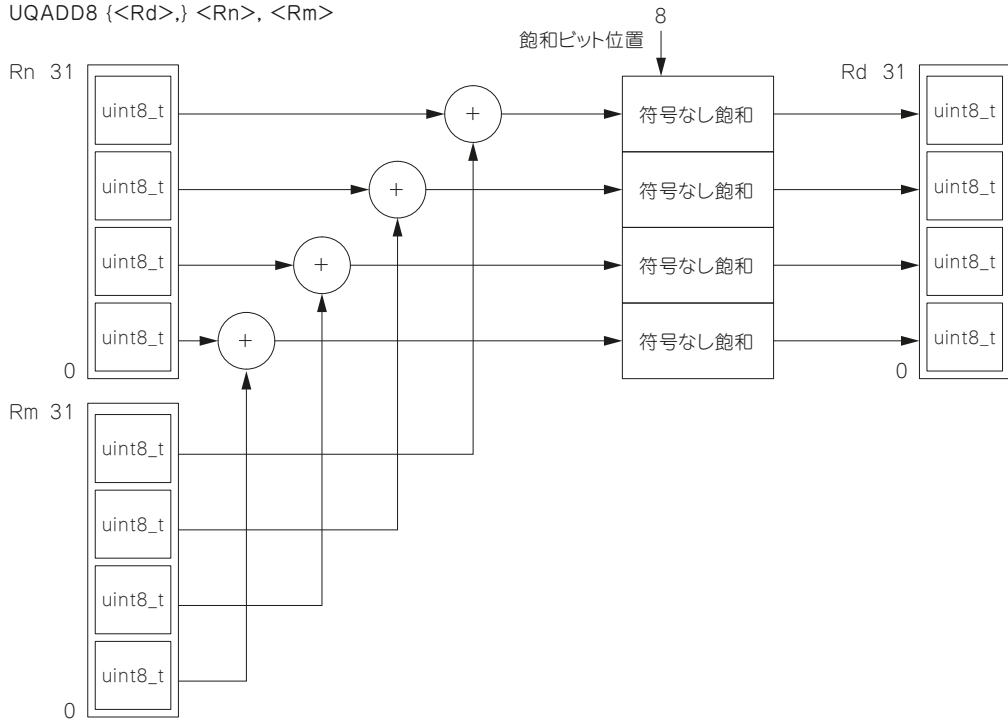
図B.83 USAT16

UQADD16 {<Rd>,} <Rn>, <Rm>



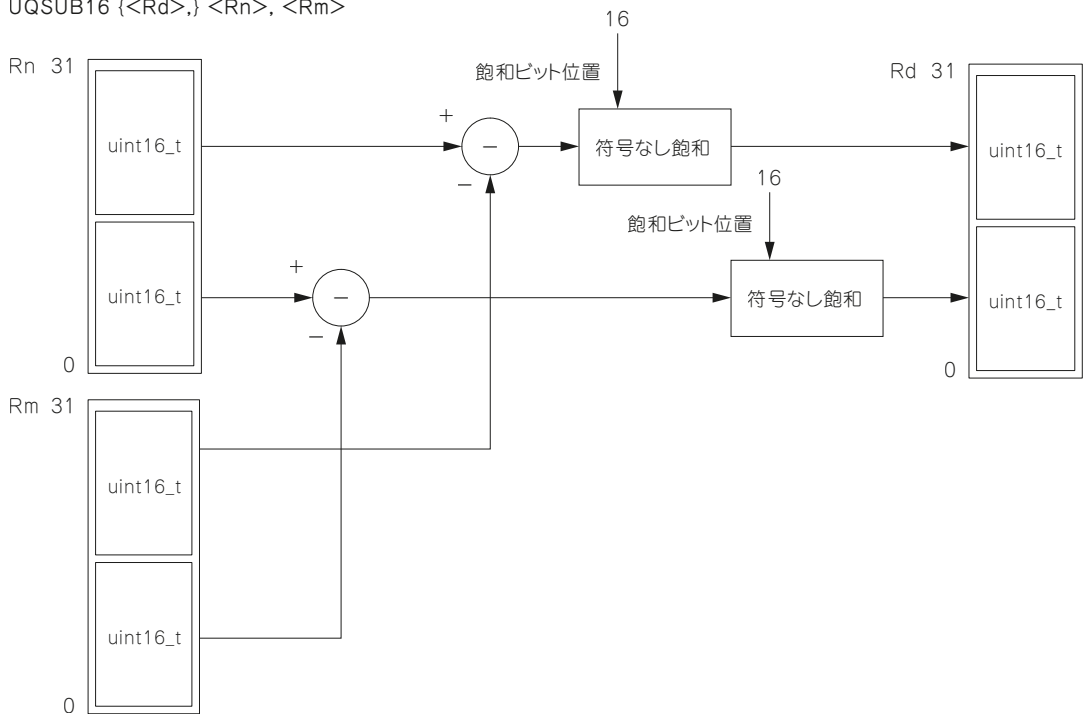
図B.84 UQADD16

UQADD8 {<Rd>,} <Rn>, <Rm>

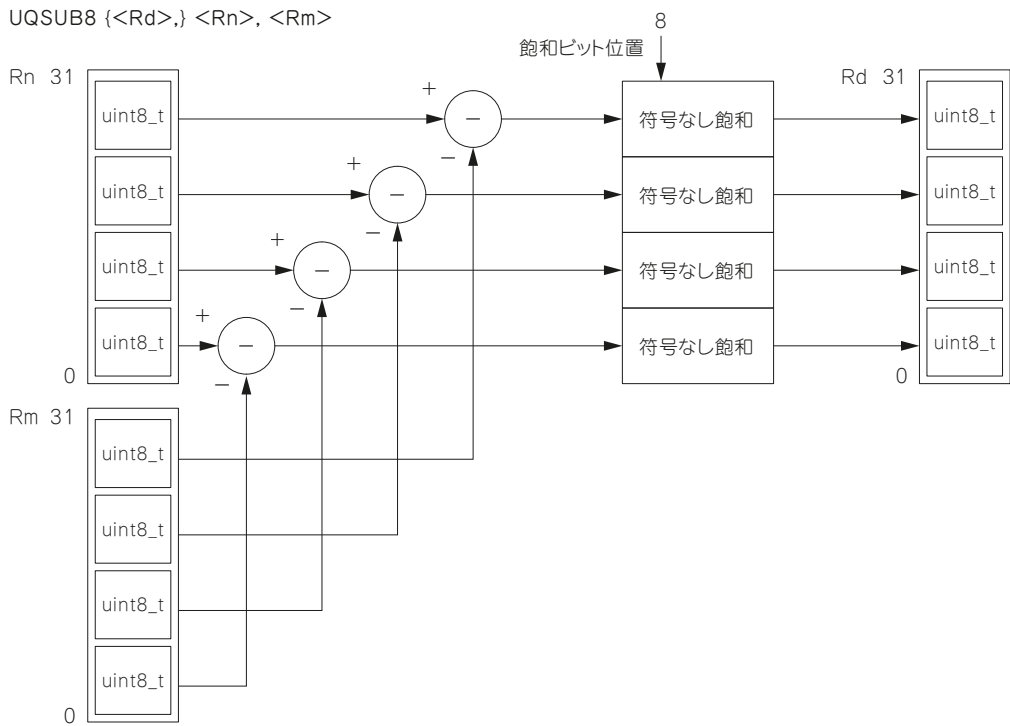


図B.85 UQADD8

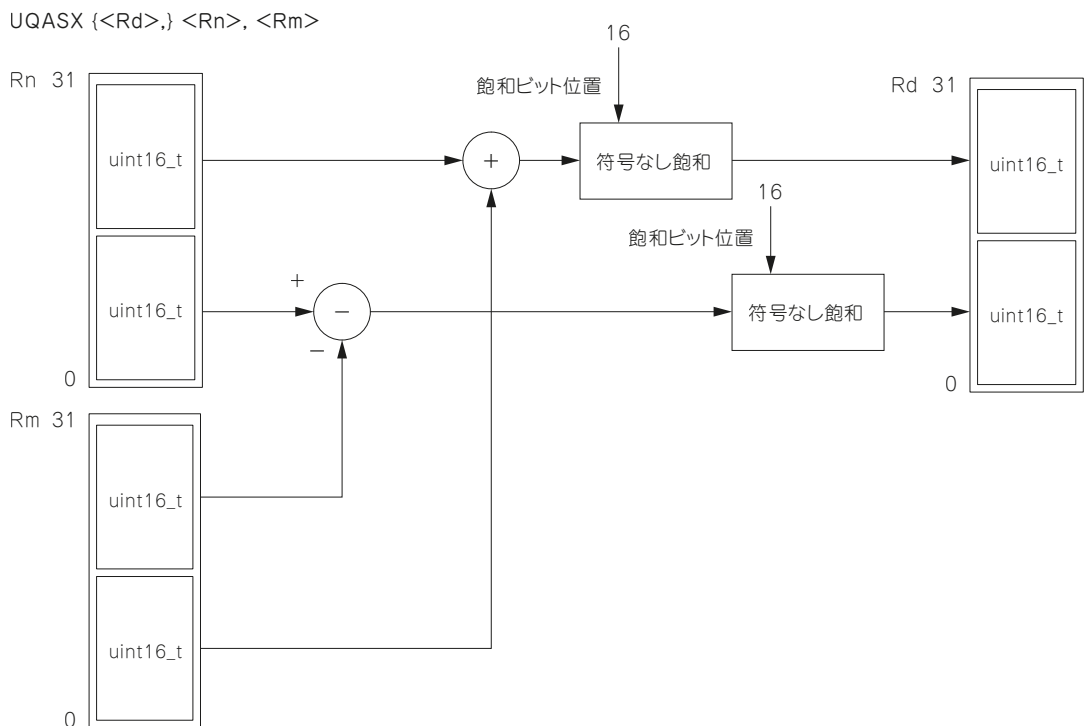
UQSUB16 {<Rd>,} <Rn>, <Rm>



図B.86 UQSUB16

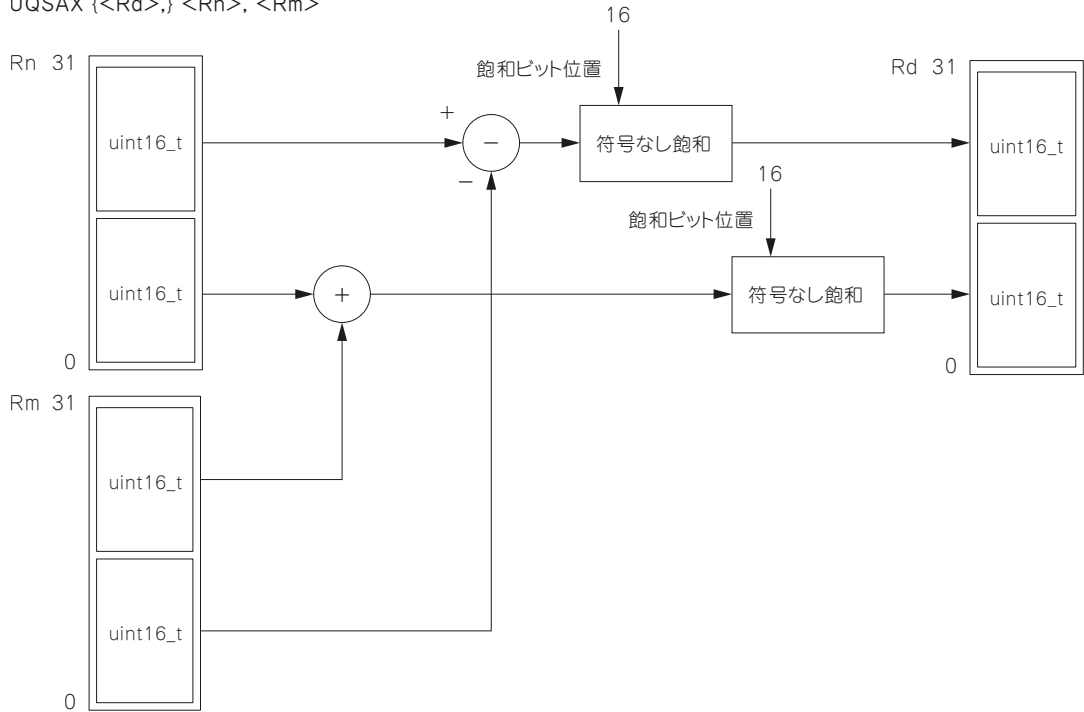


図B.87 UQSUB8



図B.88 UQASX

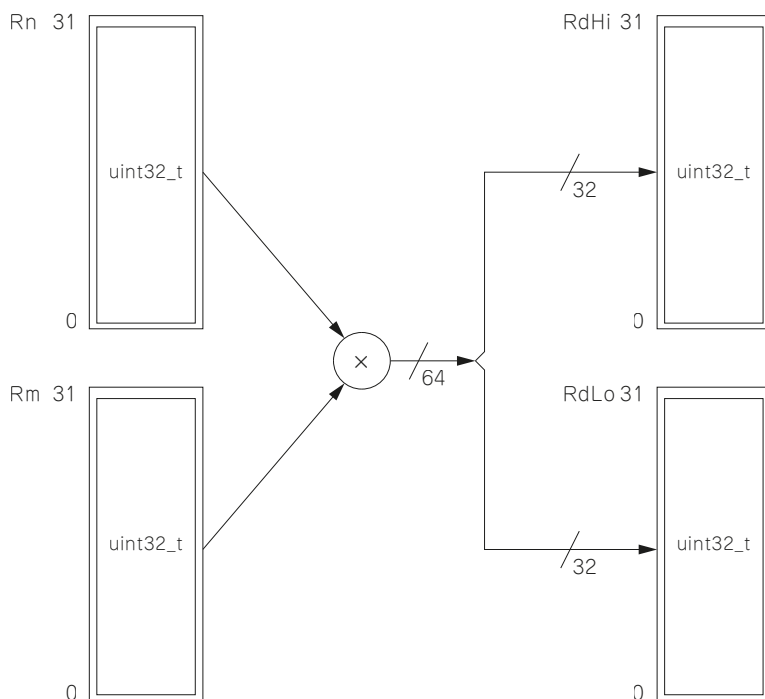
UQSAX {<Rd>,} <Rn>, <Rm>



図B.89 UQSAX

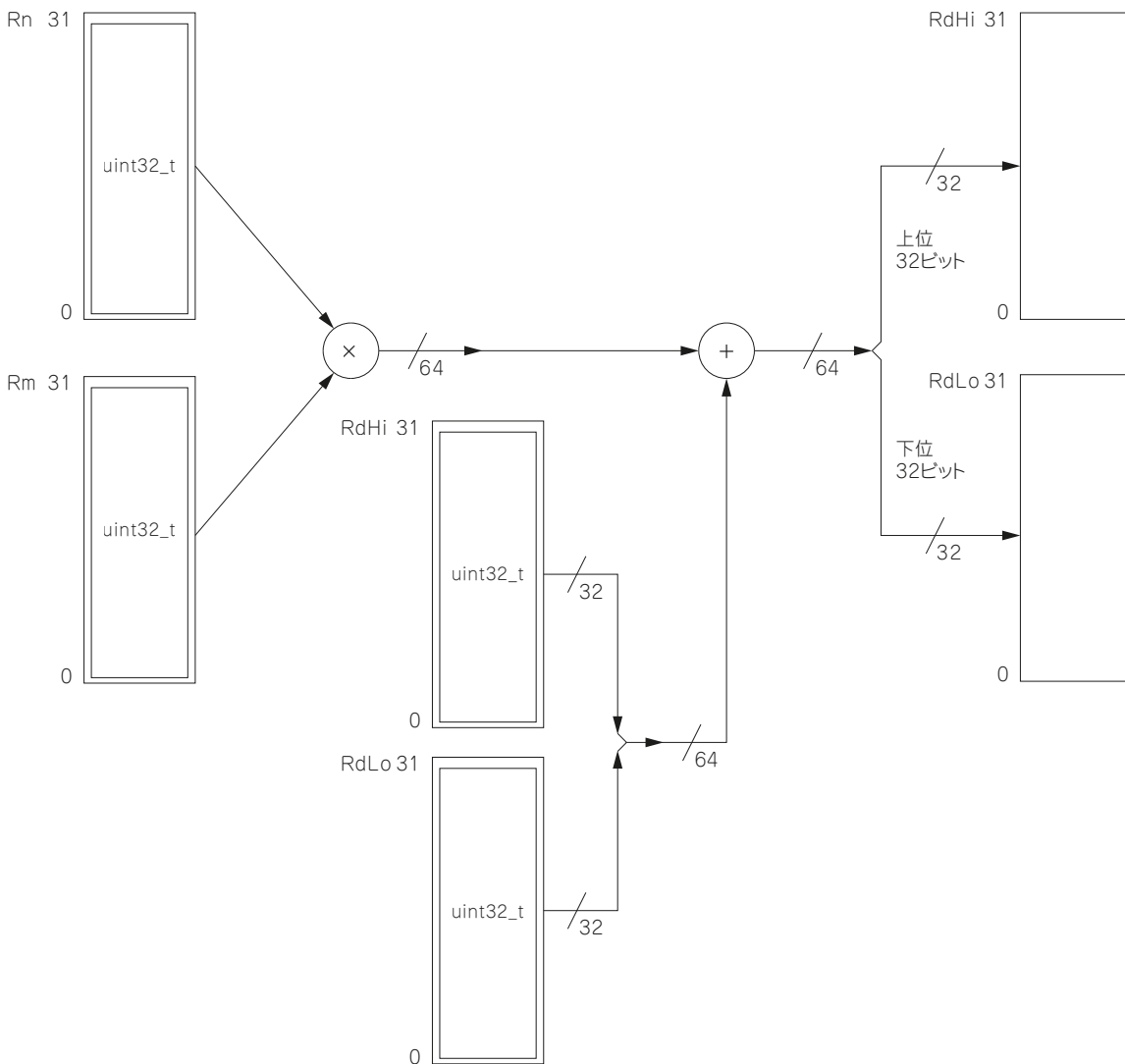
UMULL <RdLo>, <RdHi>, <Rn>, <Rm>

(DSP拡張が実装されていなくてもCortex-M33プロセッサでは利用可能)



図B.90 UMULL

UMLAL <RdLo>, <RdHi>, <Rn>, <Rm>  
 (DSP拡張が実装されていなくてもCortex-M33プロセッサでは利用可能)



図B.91 UMLAL

UMAAL <RdLo>, <RdHi>, <Rn>, <Rm>

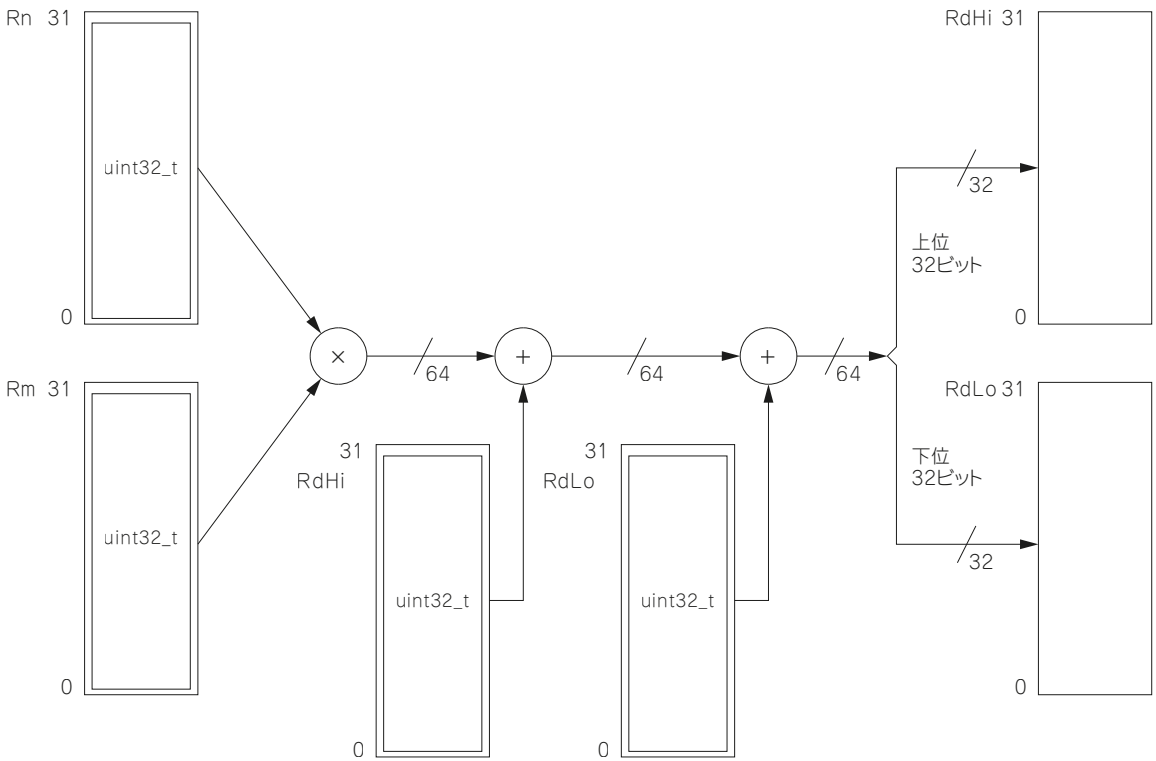


図 B.92 UMAAL

UXTB {<Rd>}, <Rn> {, ROR #imm}

(DSP拡張が実装されていなくてもCortex-M33プロセッサでは利用可能)

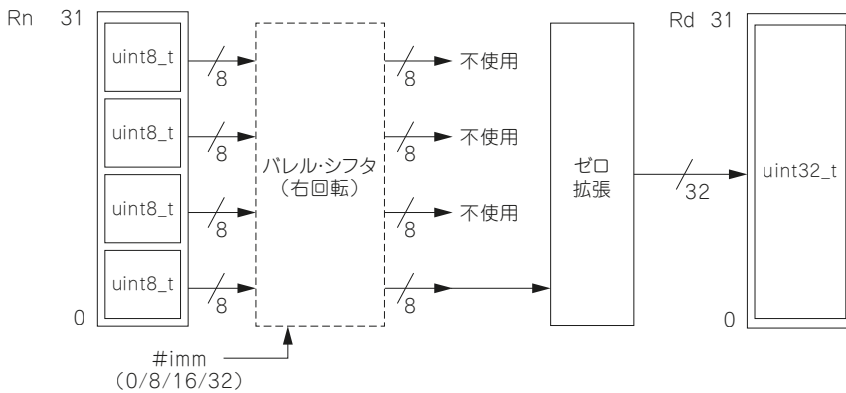
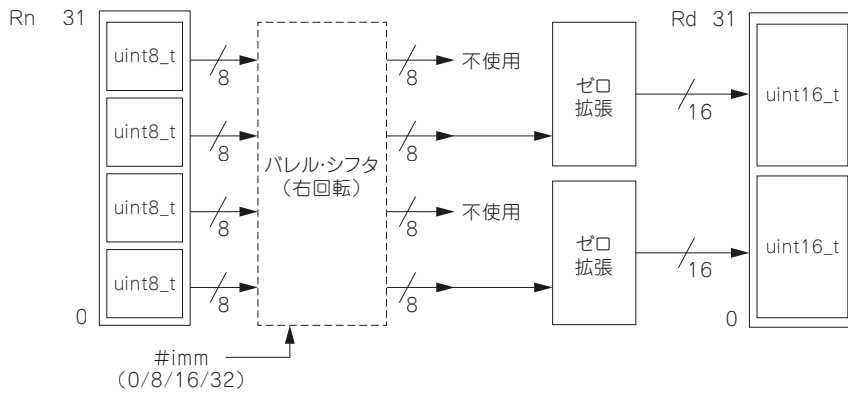


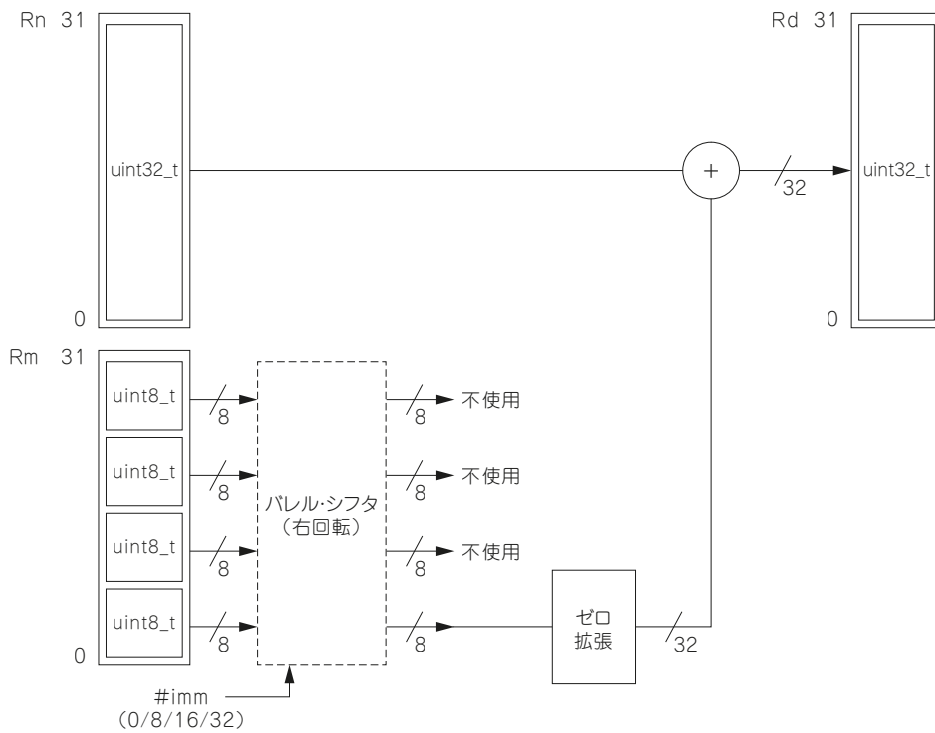
図 B.93 UXTB

UXTB16 {<Rd>}, <Rn> {, ROR #imm}



図B.94 UXTB16

UXTAB {<Rd>}, <Rn>, <Rm> {, ROR #imm}



図B.95 UXTAB

UXTAB16 {<Rd>}, <Rn>, <Rm> {, ROR #imm}

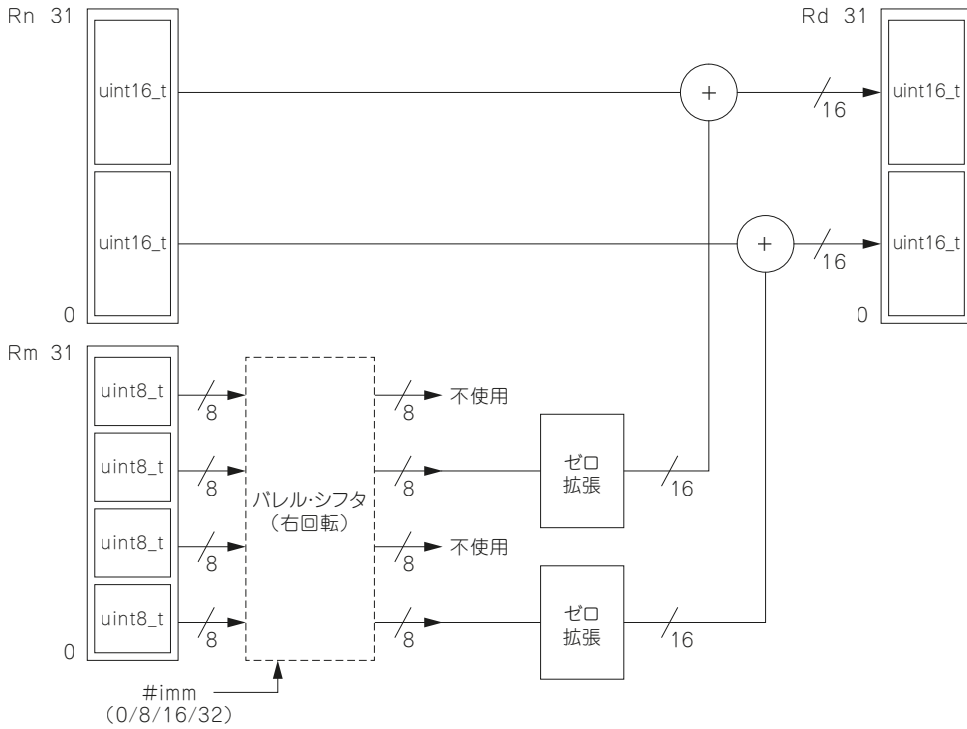


図 B.96 UXTAB16

UXTH {<Rd>}, <Rn>, <Rm> {, ROR #imm}

(DSP拡張が実装されていなくてもCortex-M33プロセッサでは利用可能)

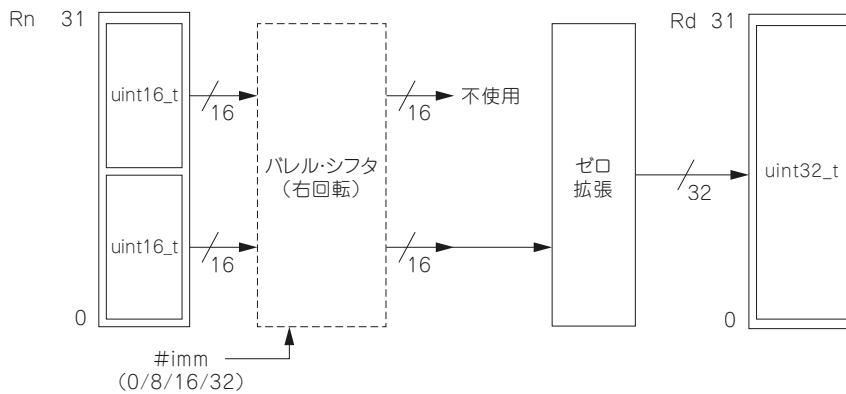


図 B.97 UXTH

UXTAH {<Rd>,} <Rn>, <Rm> {, ROR #imm}

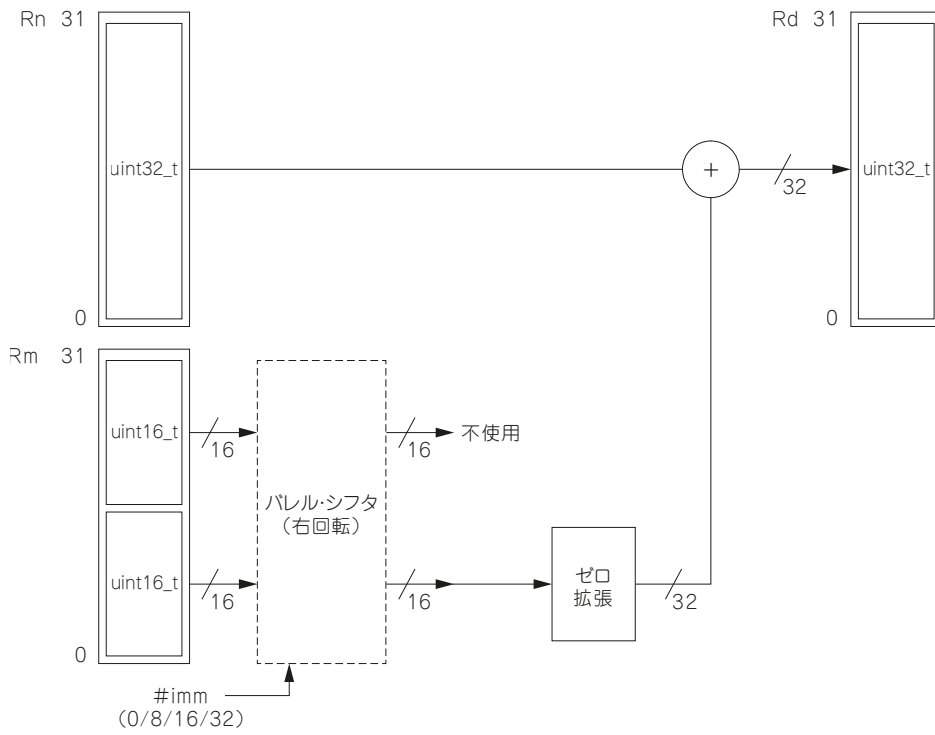


図 B.98 UXTAH